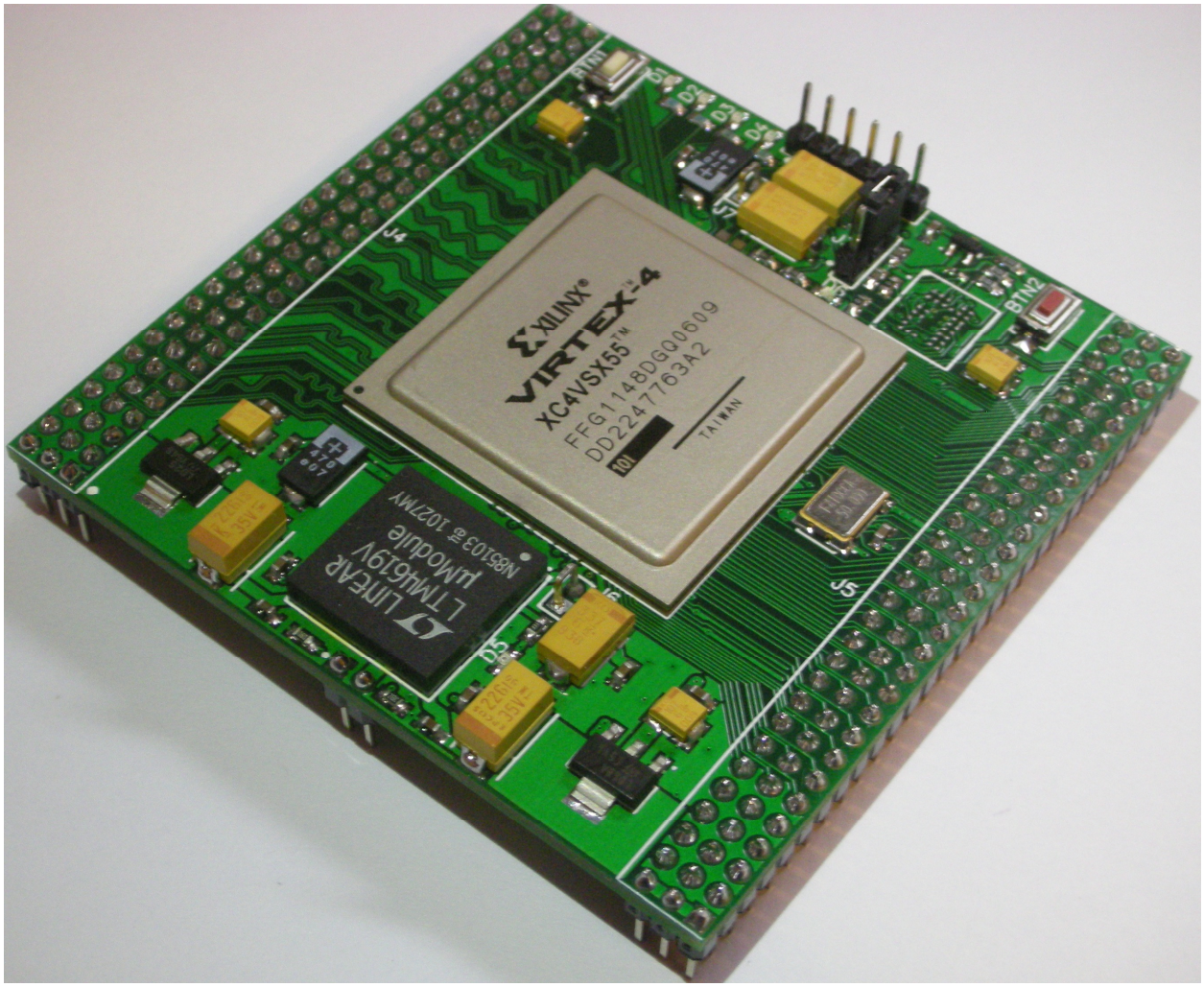
XILINX VIRTEX-4 FPGA MODULE USER's GUIDE

MODEL: XMF4-55-32 50M Revision A



Introduction

XILINX VIRTEX-4 XMF4 FPGA module is a low cost, powerful and easy to use tool. Designed for rapid prototyping and implementing FPGA designs. Board can be used for educational purposes. It can work independently, or can be used as control module in the bigger design.

Features

1) XILINX XC4VSX55 FPGA
- 55296 Logic Cells
- 512 XtremeDSP Slices
- 320x 18Kb RAM blocks (5760Kb, 500MHz)
- 8 Digital Clock Managers
- 640 User I/O (182 routed on this board)

2) XILINX XCF32P FLASH
- 32Mbit Platform Flash PROM
- IEEE Standard 1149.1/1532 Boundary-Scan (JTAG) support for programming
- Endurance of 20000 Program/Erase Cycles

3) Onboard IO peripherals
- 50MHz CMOS oscillator
- 4 LEDs
- 1 push button

4) Handy configuration
- Standard 2.54mm JTAG header
- Mode select jumper (JTAG or FLASH)
- DONE LED
- Push button for manual initiation of configuration process
- Reset supervision by voltage monitor

5) Onboard power supply
- 3.3V 4A (IO, PERIPHERALS)
- 2.5V 0.8A (VCCAUX)
- 1.2V 4A (CORE VOLTAGE)
- 1.8V 1A (Platform FLASH)
- Input voltage range 6V – 15V
- POWER-GOOD LED
- J6 and J7 jumpers to use external I/O voltage 1.14V-3.45V

6) 168 independent I/O routed to the connectors
- J4 3x29 male pin connector (84 IO, 3 GND)
- J5 3x29 male pin connector (84 IO, 3 VCC)
- 2.54mm pitch for all connectors
- 1.14V-3.45V External I/O voltage can be used
- 41 differential pairs
- Small 74x74mm PCB designed to fit on the prototyping board with 2.54mm pitch

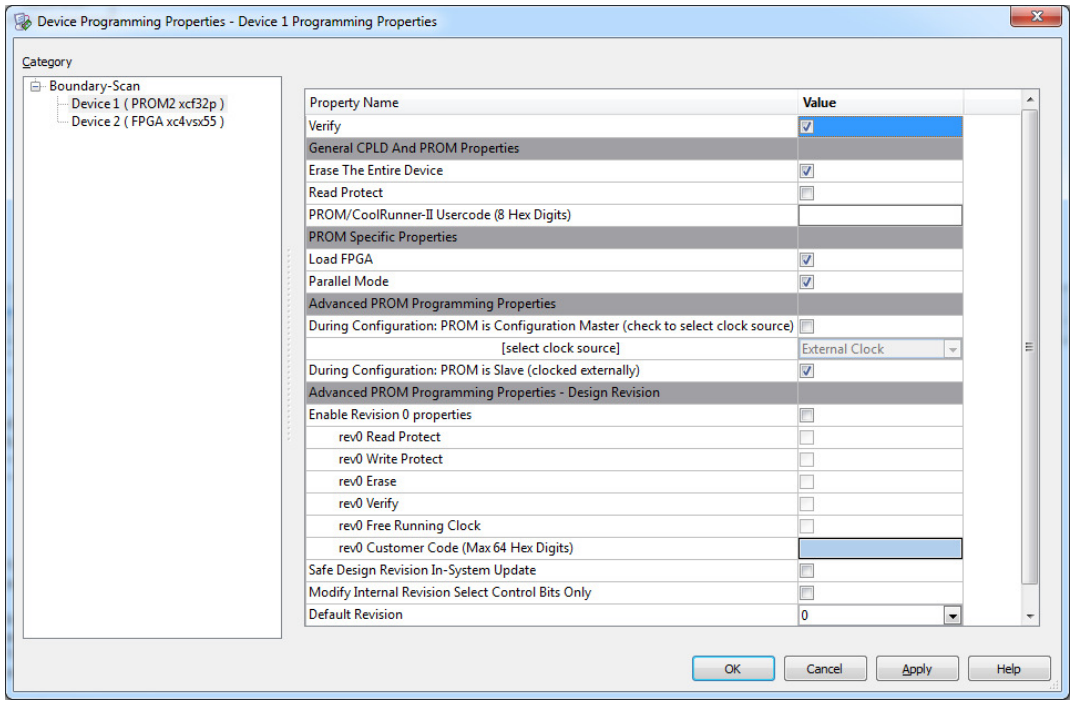
Instructions

1) Combining Advanced Silicon Modular Block (ASMBL™) architecture with a wide variety of flexible features, the Virtex®-4 family from Xilinx greatly enhances programmable logic design capabilities, making it a powerful alternative to ASIC technology. This board has XC4VSX55 FFG1148 10I FPGA (1148 ball package, speed grade 10, industrial temperature range -40°C to +100°C)

- Virtex-4 Family Overview:
  http://www.xilinx.com/support/documentation/data_sheets/ds112.pdf
- Virtex-4 FPGA DC and Switching Characteristics:
  http://www.xilinx.com/support/documentation/data_sheets/ds302.pdf
- Virtex-4 FPGA User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug070.pdf
- Virtex-4 FPGA Configuration User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug071.pdf
- XtremeDSP for Virtex-4 FPGAs User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug073.pdf

2) XILINX XCF32P is 32 Mbit platform Flash PROM with JTAG interface. Demo design will be stored to flash during manufacturing. With this demo, module functions can be tested.

XCF32P is wired in parallel mode, following iMPACT configuration should be used:



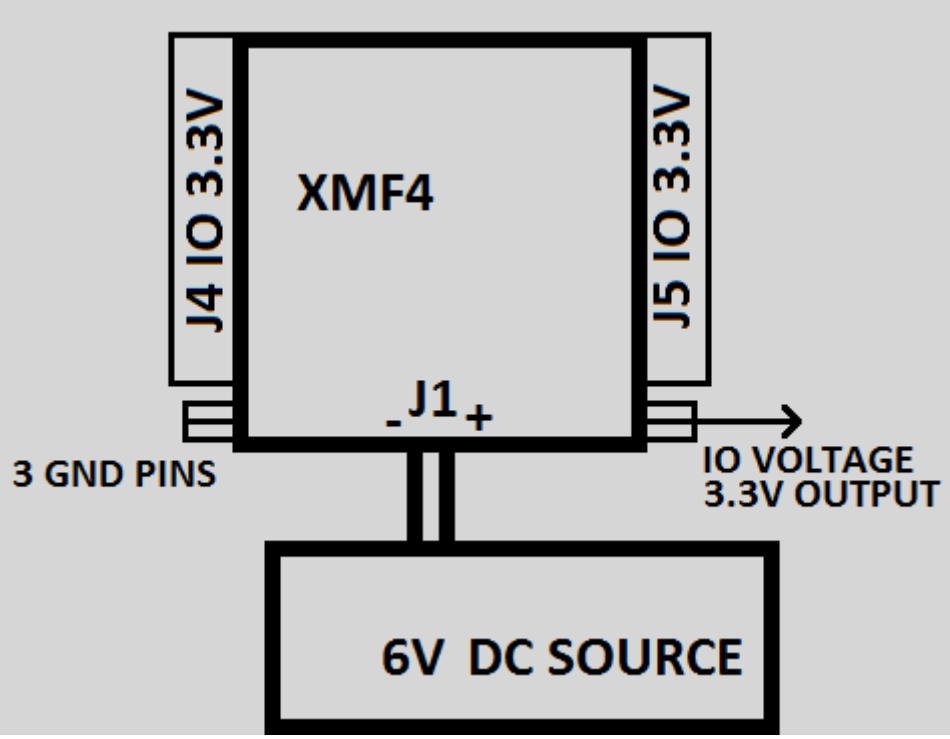
- Platform flash PROM user guide:
  http://www.xilinx.com/support/documentation/user_guides/ug161.pdf

3) Board has few simple peripherals: 4 yellow LEDs, active-low push button, and 50 MHz CMOS crystal oscillator. You can use DCM to divide or multiply clock frequency.
Additional clock signals can be connected from outside.

4) XMF4 FPGA module can be programmed via J2 JTAG header with external JTAG programmer. Red button BTN2 is connected to FPGA PROGRAM_B signal. When it is pressed – FPGA is forced to start reconfiguration process. PROGRAM_B also can be pulled low by U4, MAX809TEUR voltage monitor.
D6 is FPGA DONE LED. It turns on, after FPGA has finished configuration process.
J3 is for setting FPGA mode. When jumper is in position "FLASH MODE", this is Master SelectMAP mode (loading from flash). When jumper is in position "JTAG MODE", this is JTAG mode (waiting configuration from JTAG, not loading from the flash).
To configure or reconfigure FPGA from FLASH, set J3 jumper to "FLASH MODE", and press BTN2.
To clear FPGA configuration, and put it in JTAG mode – set J3 jumper to "JTAG MODE", and press BTN2.

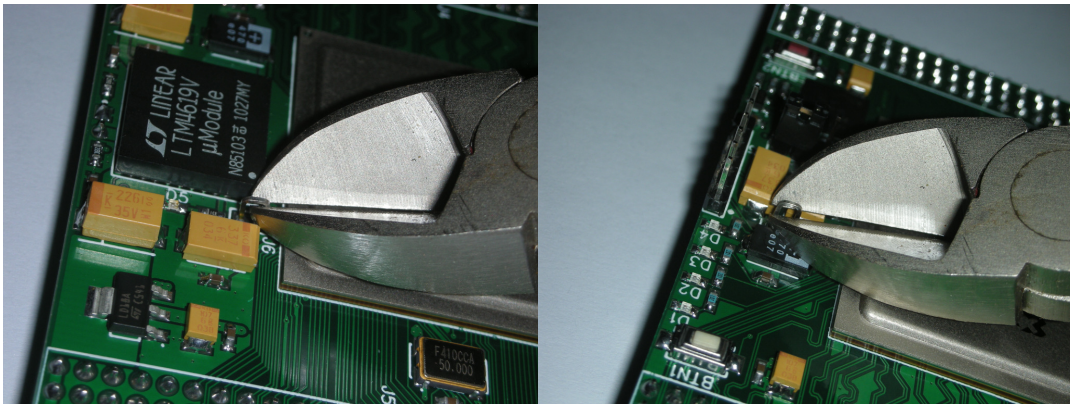
5) Board has compact power supply, to serve the needs of VIRTEX-4 FPGA. Core voltage 1.2V, and IO voltage 3.3V are provided by LTM4619V DC-DC converter. Together with tantalum capacitors, it is stable, accurate, and powerful solution. LTM4619V can deliver up to 4A current for FPGA core, and up to 4A current for IO. By default, 3.3V is used by boards peripherals and by FPGA IO. When J6 and J7 jumpers are intact, 3.3V is delivered to FPGA and J5. If J6 and J7 are cut away, then, external IO voltage should be connected to J5. Allowed IO voltage range is 1.14V-3.45V. If the upper voltage limit is breached, the FPGA IC will be permanently damaged.

Default IO voltage configuration:

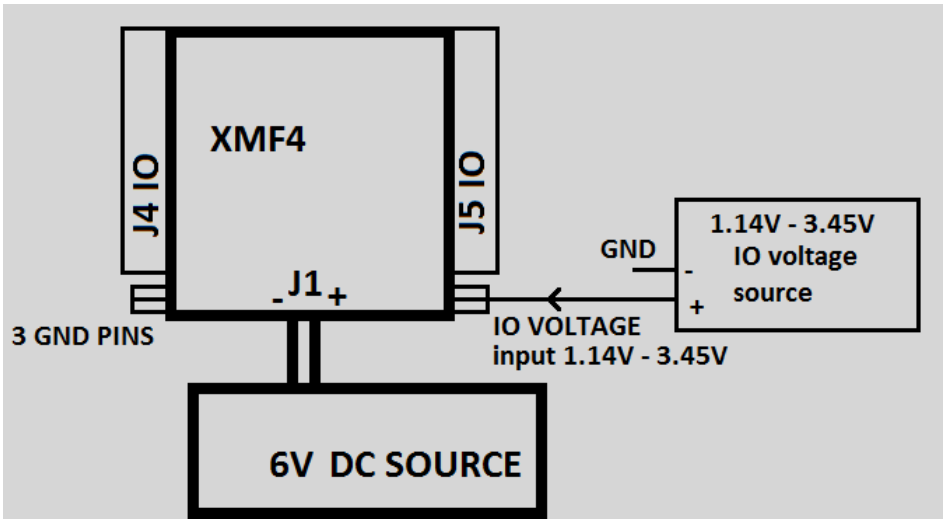


If you need to use XMF4 with IO voltage, what is not 3.3 volt:

Cut J6 Cut J7



Connect external IO voltage 1.14V-3.45V, to J5:



2.5V supply, what is used for FPGA VCCAUX, is produced by U6, 0.8A LDO.
1.8V supply, what is used for flash core voltage, is produced by U7, 1A LDO.
J1 input power voltage must be within range of 6V to 15V. There must be at least 0.5A current, to start the board with demo design. Much bigger current may be required, for your custom FPGA design. D5 is a POWER-GOOD LED, with red color. When it is on, it means that 1.2V and 3.3V voltages are within ±7.5% of the regulation point.

6) There are total 168 independent I/O pins, what are routed to the connectors, and can be used in your design. Please refer to the board schematics, to get information about connections. These I/O are not crossing with any module peripherals. J4 and J5 are 87-pin male arrays. J4 has 84 IO and 3 GND pins. J5 has 84 IO and 3 VCC pins.
Please note that you must use I/O standard “LVCMOS33” or “LVTTL”, when IO voltage is 3.3V. If you need to use other I/O standard, then, cut away J6 and J7, and connect external I/O voltage in range of 1.14V-3.45V. Please note that HSWAPEN FPGA pin is connected to GND, this means that when FPGA is not configured, all IO pull-up resistors are enabled.
When demo design is loaded to FPGA, IO connectors can be tested. Use fly wire, to connect IO pins one by one to J5 pin 1 (IO VCC). Test is passed, if LEDs are blinking, every time when one of IO pins is connected to VCC. If there is missing contact or short circuit between IO, LEDs will not blink. Be careful, and don’t make short circuit between VCC and GND.

Board has 41 differential IO pairs. Differential pairs can be sorted to 3 groups:
1: Length of negative track = lenght of positive track = 33mm. Only top PCB layer is used.

Negative input	Positive input
J4.86_K34 (IO_L29N_9)	J4.83_J34 (IO_L29P_9)
J4.82_H34 (IO_L22N_9)	J4.79_H33 (IO_L22P_9)
J4.80_F34 (IO_L14N_9)	J4.77_F33 (IO_L14P_9)
J4.76_E34 (IO_L8N_CC_LC_9)	J4.73_D34 (IO_L8P_CC_LC_9)
J4.71_C34 (IO_L7N_9)	J4.74_C33 (IO_L7P_9)
J4.17_E1 (IO_L8N_CC_LC_10)	J4.20_D1 (IO_L8P_CC_LC_10)
J4.13_G1 (IO_L17N_10)	J4.16_F1 (IO_L17P_10)
J4.14_J1 (IO_L23N_VRP_10)	J4.11_J2 (IO_L23P_VRN_10)

2: Length of negative track = lenght of positive track = 20mm. Only top PCB layer is used.

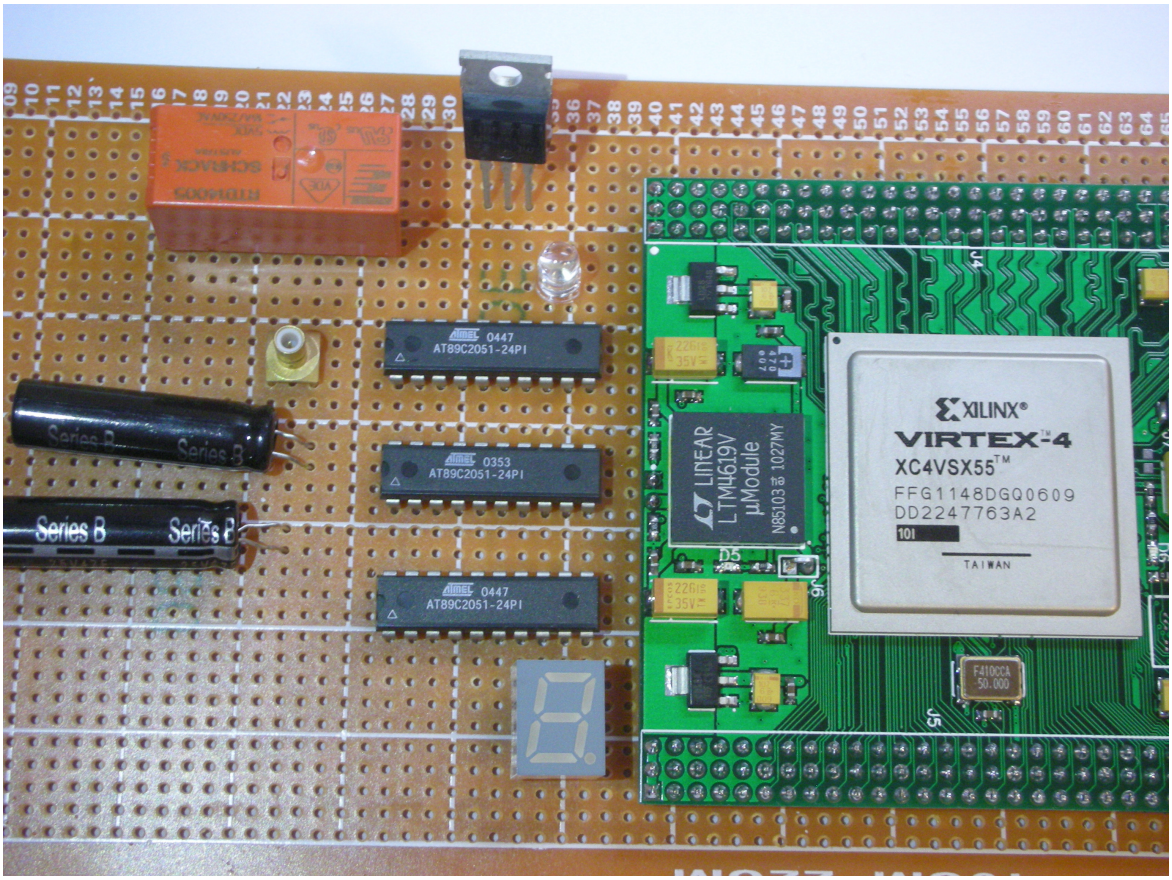
Negative input	Positive input
J4.70_B33 (IO_L31N_5)	J4.67_B32 (IO_L31P_5)
J4.65_B31 (IO_L24N_CC_LC_5)	J4.68_A31 (IO_L24P_CC_LC_5)
J4.61_B30 (IO_L18N_5)	J4.64_A30 (IO_L18P_5)
J4.62_A29 (IO_L14N_5 A29)	J4.59_A28 (IO_L14P_5)
J4.55_B26 (IO_L2N_ADC6_5)	J4.58_A26 (IO_L2P_ADC6_5)
J4.56_A25 (IO_L3N_ADC5_5)	J4.53_A24 (IO_L3P_ADC5_5)
J4.49_A21 (IO_L21N_5)	J4.52_B21 (IO_L21P_5)
J4.47_A20 (IO_L17N_CC_LC_1)	J4.50_B20 (IO_L17P_CC_LC_1)
J4.43_C18 (IO_L13N_GC_LC_1)	J4.46_C19 (IO_L13P_GC_LC_1)
J4.41_B15 (IO_L24N_LC_1)	J4.44_A15 (IO_L24P_LC_1)
J4.37_A13 (IO_L17N_6)	J4.40_A14 (IO_L17P_6)
J4.35_B11 (IO_L3N_6)	J4.38_A11 (IO_L3P_6)
J4.31_A9 (IO_L15N_6)	J4.34_A10 (IO_L15P_6)
J4.29_B8 (IO_L10N_6)	J4.32_A8 (IO_L10P_6)
J4.25_B6 (IO_L12N_VREF_6)	J4.28_A6 (IO_L12P_6)
J4.23_A3 (IO_L20N_VREF_6)	J4.26_A4 (IO_L20P_6)
J4.19_B2 (IO_L30N_6)	J4.22_B3 (IO_L30P_6)

3: Length of negative track = lenght of positive track = 50mm. Top and bottom layers are used.

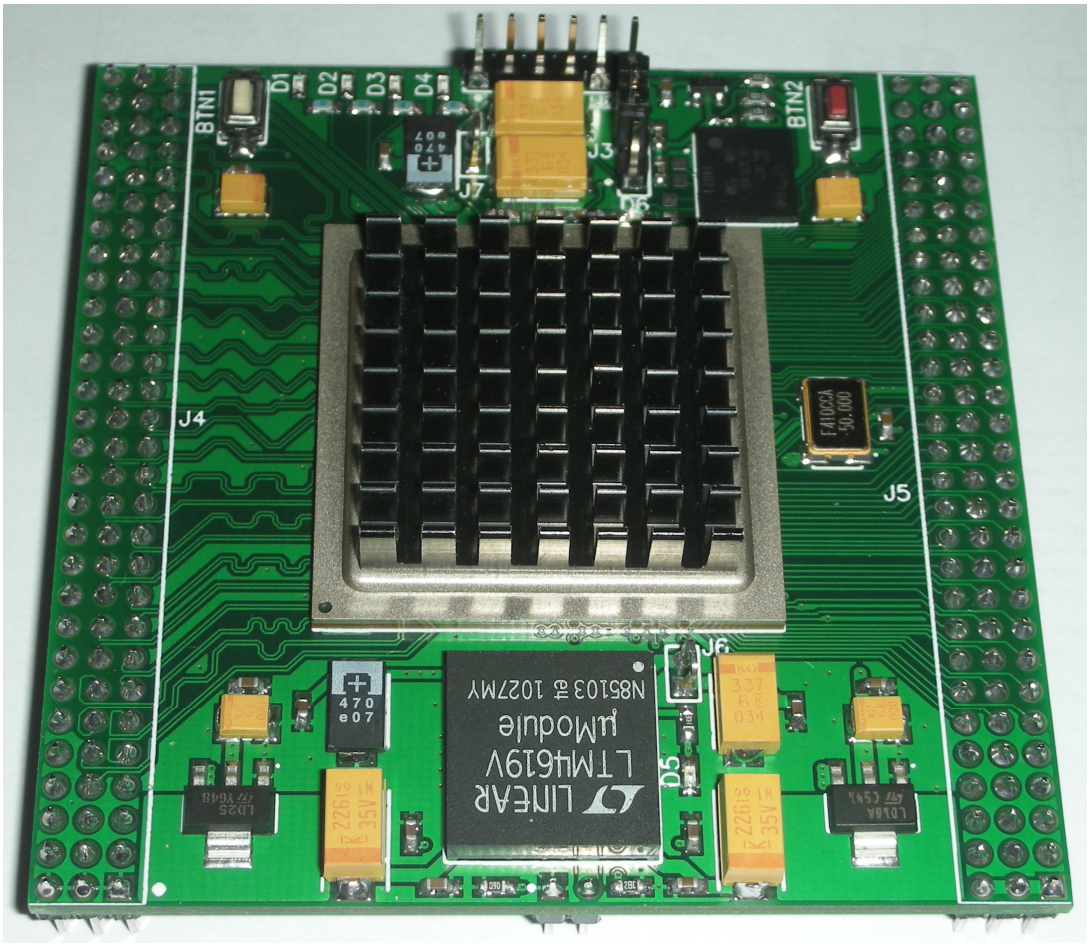
Negative input	Positive input
J4.87_K31 (IO_L23N_VRP_9)	J4.84_J31 (IO_L23P_VRN_9)
J4.81_G33 (IO_L16N_9)	J4.78_G32 (IO_L16P_9)
J4.72_D31 (IO_L26N_5)	J4.75_D30 (IO_L26P_5)
J4.69_C28 (IO_L25N_CC_LC_5)	J4.66_B28 (IO_L25P_CC_LC_5)
J4.60_A23 (IO_L1N_ADC7_5)	J4.63_B23 (IO_L1P_ADC7_5)
J4.54_C20 (IO_L15N_GC_LC_1)	J4.57_D20 (IO_L15P_GC_LC_1)
J4.48_E17 (IO_L4N_GC_VREF_LC_3)	J4.51_E18 (IO_L4P_GC_LC_3)
J4.42_F16 (IO_L6N_GC_LC_3)	J4.45_E16 (IO_L6P_GC_LC_3)
J4.39_C12 (IO_L1N_6)	J4.36_D12 (IO_L1P_6)
J4.30_C8 (IO_L4N_VREF_6)	J4.33_C9 (IO_L4P_6)
J4.24_C7 (IO_L14N_6)	J4.27_B7 (IO_L14P_6)
J4.18_B5 (IO_L22N_6)	J4.21_A5 (IO_L22P_6)
J4.12_C3 (IO_L1N_10)	J4.15_C4 (IO_L1P_10)
J4.7_K1 (IO_L26N_10)	J4.10_K2 (IO_L26P_10)
J4.5_M1 (IO_L29N_10)	J4.8_L1 (IO_L29P_10)
J4.9_M2 (IO_L28N_VREF_10)	J4.6_M3 (IO_L28P_10)

Some other differential FPGA IO are routed on this board, but PCB tracks are not matched, and not aligned, please check the schematics, if you need to locate these tracks.

All connectors have 2.54mm pitch. Board size is quite small – 74mm x 74mm. It is designed to fit on the prototyping board with 2.54mm pitch.



With some designs, FPGA can heat quite fast. Adhesive heatsink can be mounted on top of FPGA.



Model name chart