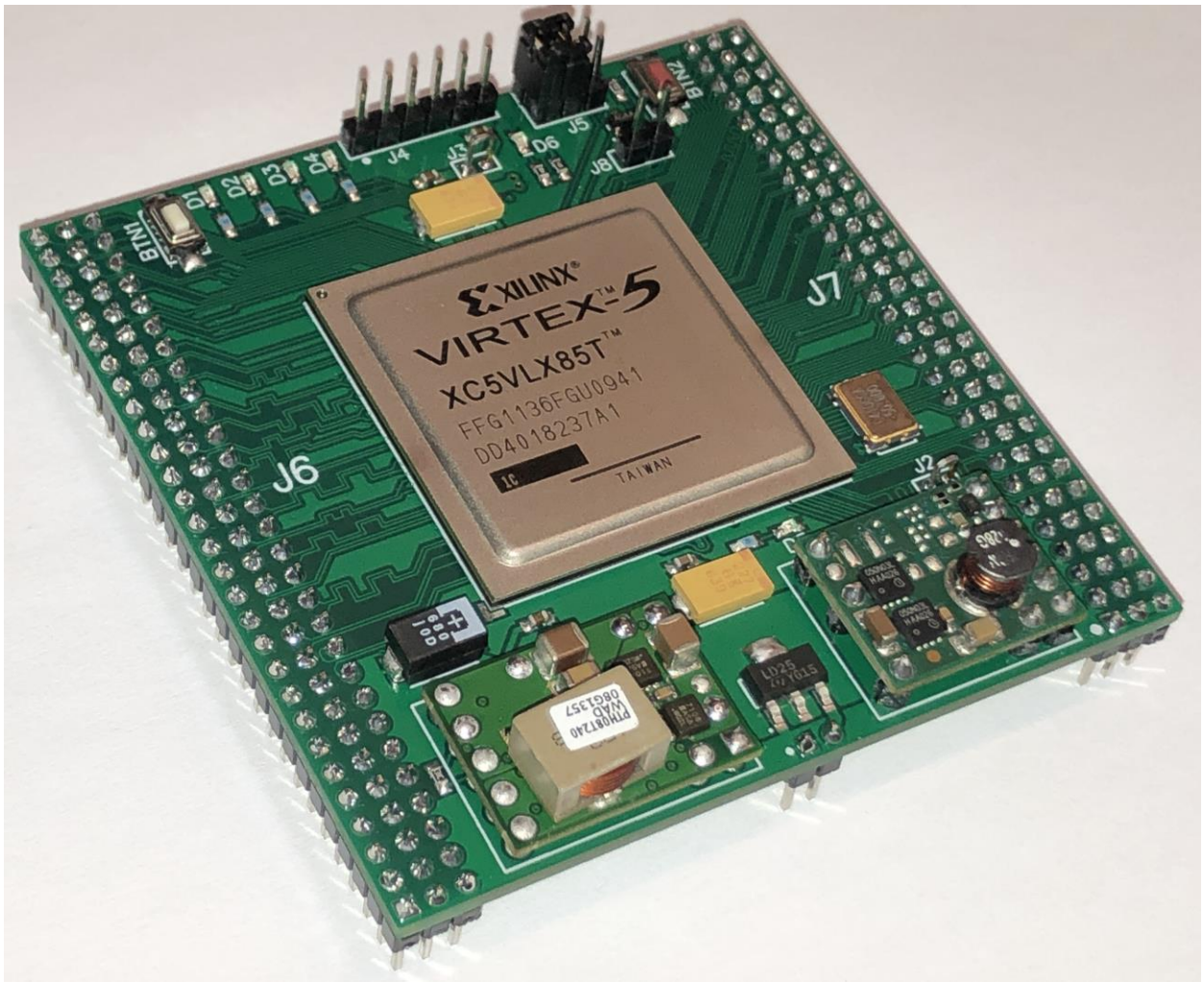
XILINX VIRTEX-5 FPGA MODULE USER's GUIDE

MODEL: XM2F5-85-256 50M Revision B



Introduction

XILINX VIRTEX-5 XM2F5 FPGA module is a powerful and easy to use tool. Designed for rapid prototyping and implementing FPGA designs. Board can be used for educational purposes. It can work independently, or can be used as control module in the bigger design.

Features

1) XILINX XC5VLX85T FPGA
- 12960 Virtex-5 Slices (82994 Logic Cells)
- 48x DSP48E Slices
- 108x 36Kb RAM blocks (3888Kb, 550MHz)
- 6 Clock Management Tiles
- 480 User I/O (217 routed on this board)

2) SPANSION S29GL256P10 FLASH
- 256Mbit
- BPI Interface
- FPGA configuration
- Post-configuration access
- 100,000 erase cycles per sector typical
- 20-year data retention typical

3) Onboard IO peripherals
- 50MHz CMOS oscillator
- 4 LEDs
- 1 push button

4) Handy configuration
- Standard 2.54mm JTAG header
- Mode select jumpers
- DONE LED
- Push button for manual initiation of configuration process
- Header for external reset
- Reset supervision by voltage monitor

5) Onboard power supply
- 3.3V 6A (IO, PERIPHERALS)
- 2.5V 0.8A (VCCAUX)
- 1V 10A (CORE VOLTAGE)
- Input voltage range 5V – 14V
- POWER-ON LED
- J2 and J3 jumpers to use external I/O voltage 1.14V-3.45V

6) 168 independent I/O routed to the connectors
- J6 3x29 male pin connector (84 IO, 3 GND)
- J7 3x29 male pin connector (84 IO, 3 VCC)
- 2.54mm pitch for all connectors
- 1.14V-3.45V External I/O voltage can be used
- 17 differential pairs
- Small 74x74mm PCB designed to fit on the prototyping board with 2.54mm pitch

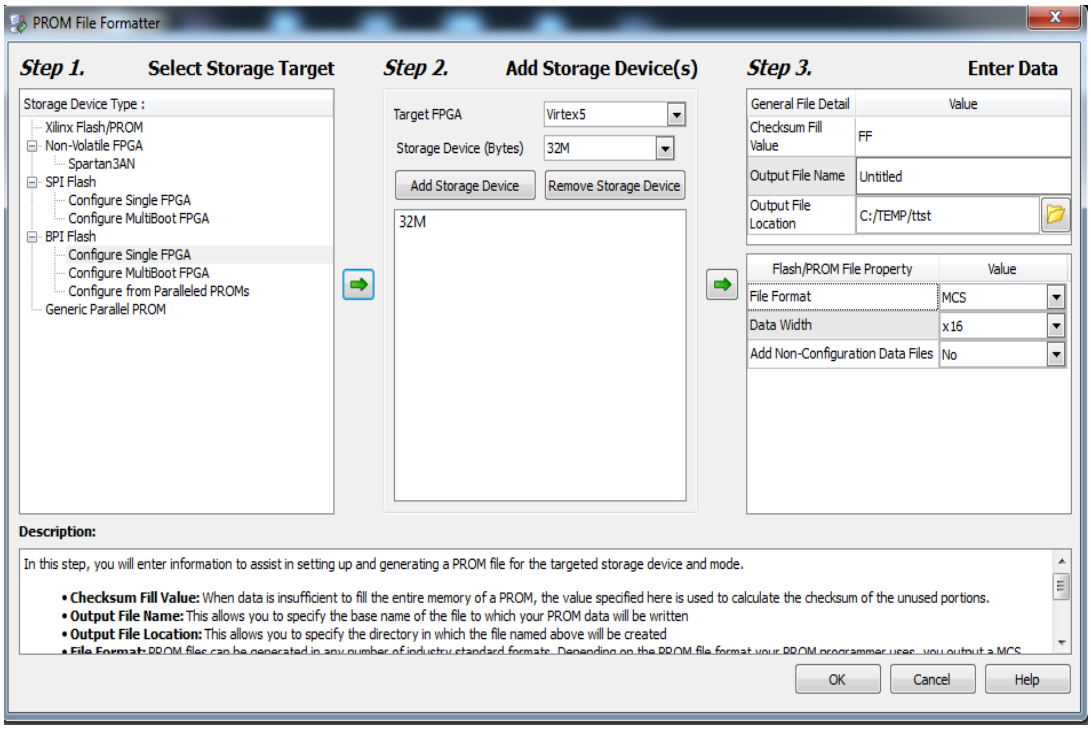
Instructions

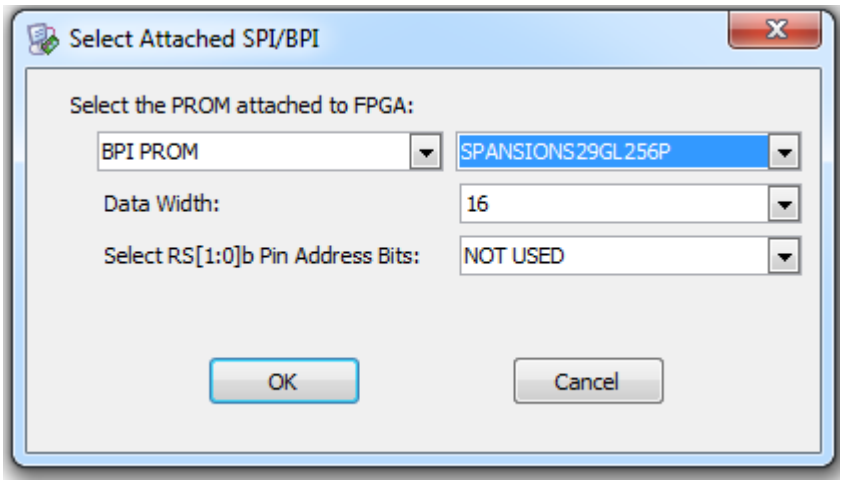
1) The Virtex-5 family provides powerful features in the FPGA market. In addition to the advanced, high-performance logic fabric, Virtex-5 FPGAs contain many hard-IP system level blocks. These features allow advanced logic designers to build the highest levels of performance and functionality into their FPGA-based systems. Built on a 65-nm state-of-the-art copper process technology, Virtex-5 FPGAs are a programmable alternative to custom ASIC technology. This board has XC5VLX85T FF1136 1C FPGA (1136 ball package, speed grade 1, commercial temperature range 0°C to +85°C.

- Virtex-5 Family Overview:
  http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
- Virtex-5 FPGA User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
- Virtex-5 FPGA XtremeDSP Design Considerations:
  http://www.xilinx.com/support/documentation/user_guides/ug193.pdf

2) SPANSION S29GL256P10 is 256 Mbit Page Flash with 90 nm MirrorBit Process Technology. Demo design will be stored to flash during manufacturing.
With this demo, module functions can be tested.

S29GL256P10 is wired in parallel mode, following iMPACT configuration should be used:





- SPANSION S29GL256P10 datasheet:
  https://www.cypress.com/file/219926/download
- Indirect Programming of BPI PROMs with Virtex-5 FPGAs:
  https://www.xilinx.com/support/documentation/application_notes/xapp973.pdf

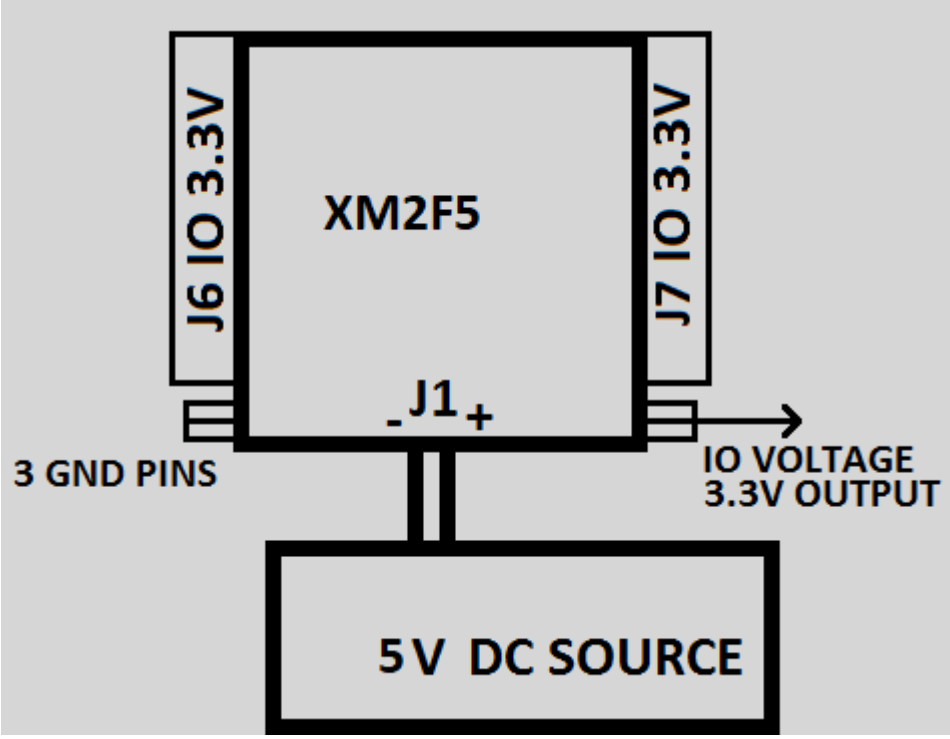
3) Board has few simple peripherals: 4 yellow LEDs, active-low push button, and 50 MHz CMOS crystal oscillator. You can use DCM to divide or multiply clock frequency.
Additional clock signals can be connected from outside.

4) XM2F5 FPGA module can be programmed via J4 JTAG header with external JTAG programmer. Red button BTN2 is connected to FPGA PROGRAM_B signal. When it is pressed – FPGA is forced to start reconfiguration process. PROGRAM_B also can be pulled low by U5, MAX809TEUR voltage monitor. This module has J8 connector, what is connected in parallel to BTN2.
J8 can be used to reset the FPGA module externally. To reset module externally, connect "NO" relay contacts to J8. D6 is FPGA DONE LED. It turns on, after FPGA has finished configuration process. J5 is for setting FPGA mode. When jumpers are in positions M0 and M2, this is Master BPI-Up mode (loading from flash). When jumper is in position M1 only, this is JTAG mode (waiting configuration from JTAG, not loading from the flash).
To configure or reconfigure FPGA from FLASH, set J5 jumper to Master BPI-Up mode, and press BTN2. To clear FPGA configuration, and put it in JTAG mode – set J5 jumper to JTAG mode, and press BTN2.

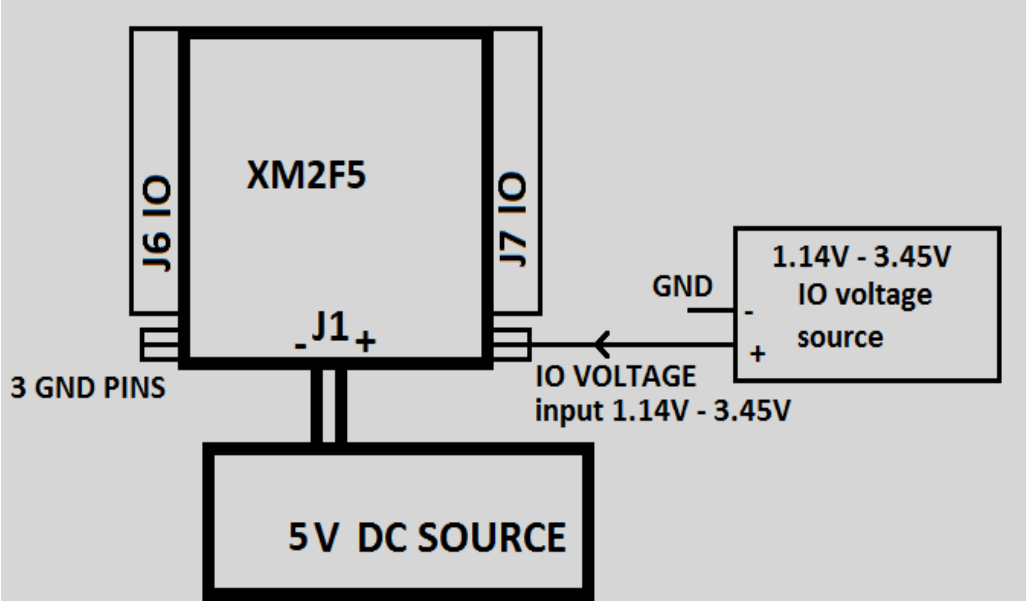
- Virtex-5 FPGA Configuration User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug191.pdf

5) Board has compact power supply, to serve the needs of VIRTEX-5 FPGA. Core voltage 1V is provided by PTH08T240, and IO voltage 3.3V is provided by PTH08T230. Together with tantalum capacitors, it is stable, accurate, and powerful solution. PTH08T240 can deliver up to 10A current for FPGA core. PTH08T230 can deliver up to 6A current for IO. By default, 3.3V is used by boards peripherals and by FPGA IO. When J2 and J3 jumpers are intact, 3.3V is delivered to FPGA and J7. If J2 and J3 are cut away, then, external IO voltage should be connected to J7. Allowed IO voltage range is 1.14V-3.45V. If the upper voltage limit is breached, the FPGA IC will be permanently damaged.

Default IO voltage configuration:



If you need to use XM2F5 module with IO voltage, what is less than 3.3 volt,
then cut J2 and J3 with nippers, and connect external IO voltage 1.14V-3.45V, to J7:



2.5V supply, what is used for FPGA VCCAUX, is produced by U2, 0.8A LDO.
J1 input power voltage must be within range of 5V to 14V. There must be at least 1A current, to start the board with demo design. Much bigger current may be required, for your custom FPGA design. D5 is a POWER-ON LED, with red color. When it is on, it means that input voltage is connected with correct polarity.

- Virtex-5 FPGA DC and Switching Characteristics:
  http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf

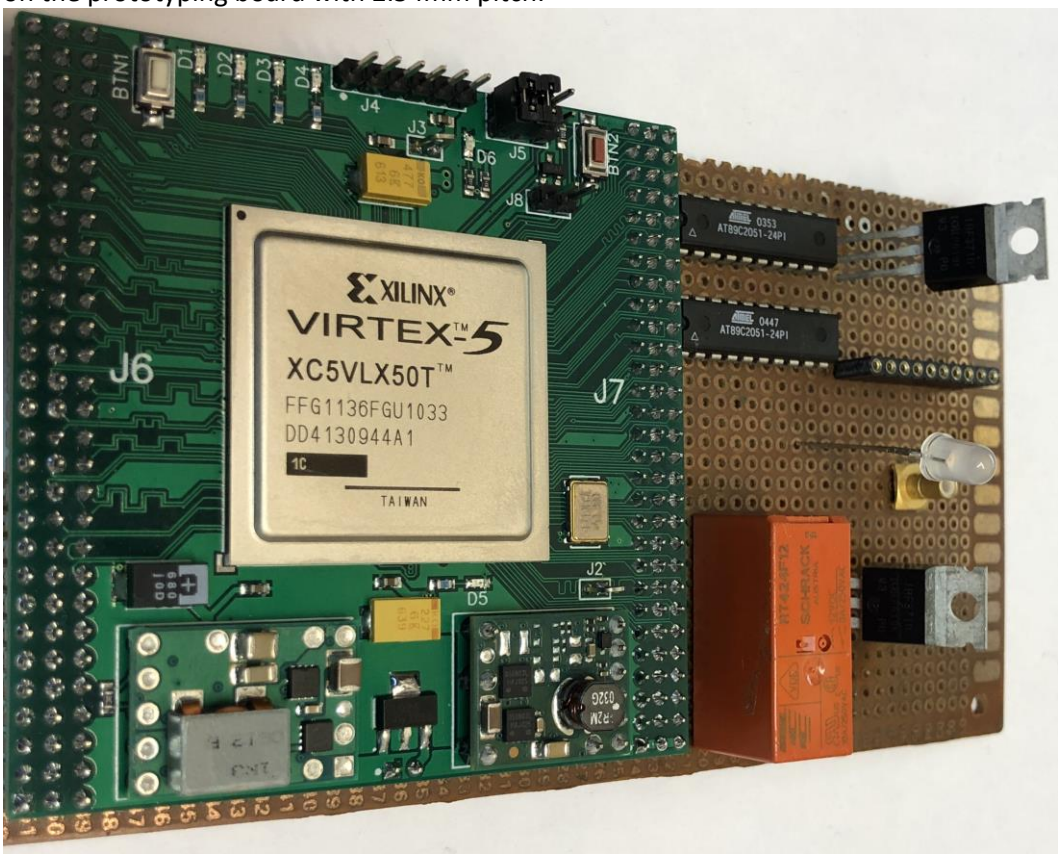
6) There are total 168 independent I/O pins, what are routed to the connectors, and can be used in your design. Please refer to the board schematics, to get information about connections. These I/O are not crossing with any module peripherals. J6 and J7 are 87-pin male arrays. J6 has 84 IO and 3 GND pins. J7 has 84 IO and 3 VCC pins.
Please note that you must use I/O standard "LVCMOS33" or "LVTTL", when IO voltage is 3.3V. If you need to use other I/O standard, then, cut away J2 and J3, and connect external I/O voltage in range of 1.14V-3.45V. Please note that HSWAPEN FPGA pin is connected to GND, this means that when FPGA is not configured, all IO pull-up resistors are enabled.
When demo design is loaded to FPGA, IO connectors can be tested. Use fly wire, to connect IO pins one by one to J7 pin 1 (IO VCC). Test is passed, if LEDs are blinking, every time when one of IO pins is connected to VCC. If there is missing contact or short circuit between IO, LEDs will not blink. Be careful, and don't make short circuit between VCC and GND.

Board has 17 differential IO pairs.
Length of negative track = lenght of positive track = 25mm. Only top PCB layer is used.

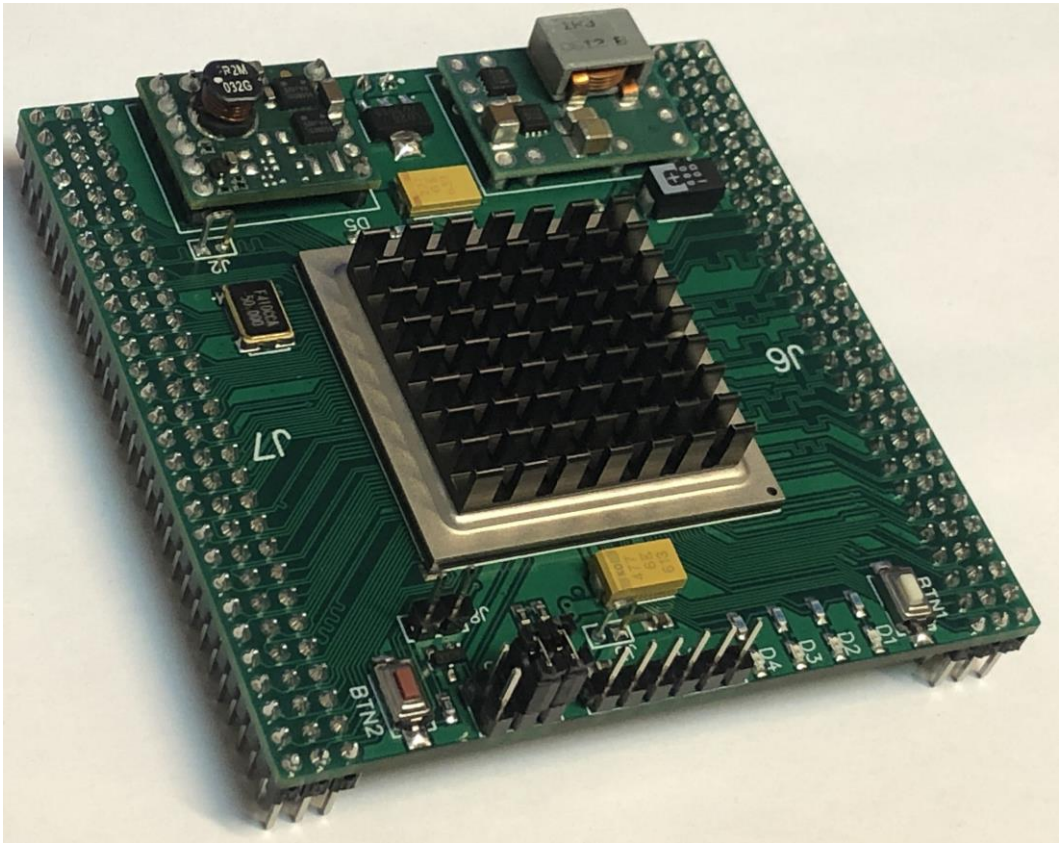
Negative input	Positive input
J6.47_U7 (IO_L10N_CC_12)	J6.50_T8 (IO_L10P_CC_12)
J6.39_AD7 (IO_L3N_18)	J6.42_AC7 (IO_L3P_18)
J6.44_Y7 (IO_L6N_18)	J6.41_AA6 (IO_L6P_18)
J6.45_Y6 (IO_L8N_CC_18)	J6.48_W6 (IO_L8P_CC_18)
J6.35_AF6 (IO_L9N_CC_18)	J6.38_AE7 (IO_L9P_CC_18)
J6.30_AK6 (IO_L18N_18)	J6.27_AK7 (IO_L18P_18)
J6.36_AF5 (IO_L10N_CC_18)	J6.33_AG5 (IO_L10P_CC_18)
J6.53_P5 (IO_L3N_12)	J6.56_N5 (IO_L3P_12)
J6.57_L5 (IO_L4N_VREF_12)	J6.60_L4 (IO_L4P_12)
J6.51_T6 (IO_L7N_12)	J6.54_R6 (IO_L7P_12)
J6.59_J5 (IO_L8N_CC_12)	J6.62_J6 (IO_L8P_CC_12)
J6.68_F6 (IO_L15N_12)	J6.65_F5 (IO_L15P_12)
J6.66_G5 (IO_L13N_12)	J6.63_H5 (IO_L13P_12)
J7.22_AP32 (IO_L19N_13)	J7.24_AN32 (IO_L19P_13)
J7.73_F34 (IO_L7N_11)	J7.74_G33 (IO_L7P_11)
J7.59_R34 (IO_L16N_SM12N_11)	J7.57_T33 (IO_L16P_SM12P_11)
J7.65_M33 (IO_L12N_VRP_11)	J7.63_N33 (IO_L12P_VRN_11)

Some other differential FPGA IO are routed on this board, but PCB tracks are not matched, and not aligned, please check the schematics, if you need to locate these tracks.

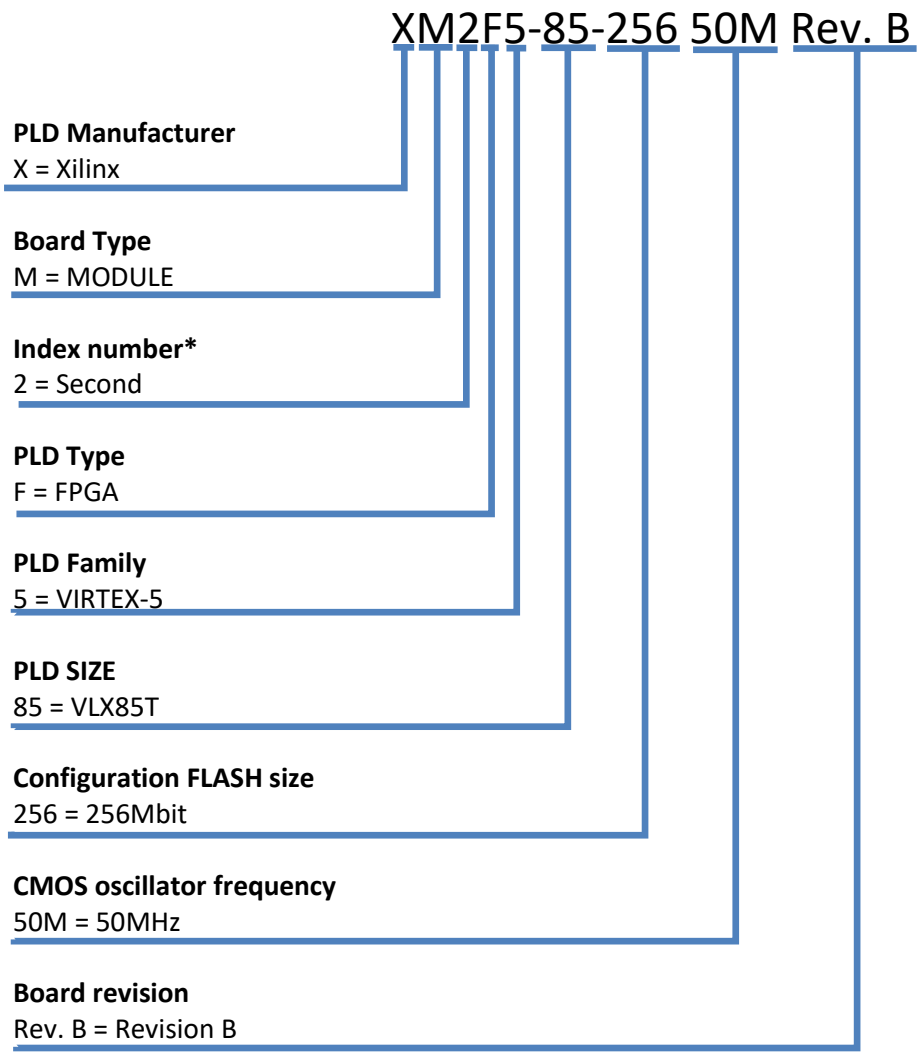
All connectors have 2.54mm pitch. Board size is quite small – 74mm x 74mm. It is designed to fit on the prototyping board with 2.54mm pitch.



With some designs, FPGA can heat quite fast. Adhesive heatsink can be mounted on top of FPGA.



Model name chart



* The index number is used to distinguish from a similar model