XILINX VIRTEX-5 FPGA KIT USER's GUIDE

MODEL: XKF5-110-512-256-16 Revision A

Introduction

Xilinx Virtex-5 XKF5 FPGA kit is designed for rapid prototyping and implementing FPGA designs. Board can be used for educational purposes. It can work independently or can be used as a control module in the bigger design.

Features

1) XILINX XC5VLX110T FFG1738 1C FPGA
- 17280 Virtex-5 Slices (110592 Logic Cells)
- 64 DSP48E Slices
- 148x 36Kb RAM blocks (5328Kb, 550MHz)
- 6 Clock Management Tiles
- 1 Endpoint Block for PCI Express
- 4 Ethernet MACs
- 16 GTP RocketIO 3.75 Gb/s Transceivers (8 routed on this board)
- 680 User I/O (299 routed on this board)

2) SPANSION S29GL512P10 FLASH
- 512Mbit
- BPI Interface
- FPGA configuration with multiboot feature
- Post-configuration access
- 100,000 erase cycles per sector typical
- 20-year data retention typical

3) Onboard IO peripherals
- 256Mbit 143MHz SDRAM
- 16Gbit NAND FLASH
- 1024Kbit EEPROM
- FTDI FT2232C USB controller
- 50MHz CMOS oscillator for IO
- 75MHz LVPECL oscillator for Rocket IO
- 125MHz LVPECL oscillator for Rocket IO
- 8 IO LEDs
- 8 DIP switches
- IO push button
- Speaker
- VGA port
- System monitor

4) RocketIO Transceivers
- 3x SATA HOST port
- 3x SATA TARGET port
- One MGT clock input routed to SMA connectors
- Two transceivers routed to 1.27mm male header

5) Handy configuration
- Configuration from onboard USB programmer
- Configuration from external programmer
- Mode select jumpers
- DONE LED

- Flash busy LED
- Push button for manual initiation of configuration process
- Header for external reset
- Reset supervision by voltage monitor

6) Onboard power supply
- 5V 1.5A (USB controller)
- 3.3V 6A (IO, PERIPHERALS)
- 2.5V 1.5A (VCCAUX)
- 1V 30A (CORE VOLTAGE)
- 1.2V 3A (Rocket IO)
- Input voltage range 11V – 13V
- POWER-ON LED
- AUX input for I/O voltage 1.14V-3.45V

7) 138 I/O routed to the connectors
- Two 5x13 male pin arrays (130 IO) with selectable IO voltage
- One 2x6 female connector (8 IO, 2 GND, 2 VCC 3.3V)
- Peripheral modules support
- 2.54mm pitch for all connectors
- I^2C header
- NAND FLASH header

8) Small 100x100mm PCB with M3 mounting holes

Instructions

1) The Virtex-5 family provides the newest most powerful features in the FPGA market. In addition to the most advanced, high-performance logic fabric, Virtex-5 FPGAs contain many hard-IP system level blocks. These features allow advanced logic designers to build the highest levels of performance and functionality into their FPGA-based systems. Built on a 65-nm state-of-the-art copper process technology, Virtex-5 FPGAs are a programmable alternative to custom ASIC technology. This board has XC5VLX110T FFG1738 1C FPGA (1738 ball package, speed grade 1, commercial temperature range 0°C to +85°C.

- Virtex-5 Family Overview:
  http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
- Virtex-5 FPGA DC and Switching Characteristics:
  http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf
- Virtex-5 FPGA User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
- Virtex-5 FPGA XtremeDSP Design Considerations:
  http://www.xilinx.com/support/documentation/user_guides/ug193.pdf

2) SPANSION S29GL512P10 is 512 Mbit Page Flash with 90 nm MirrorBit Process Technology. Demo design will be stored to flash during manufacturing. With this demo, all board functions can be tested. Demo design also includes a BPI multiboot feature.

Following iMPACT configuration should be used:

- SPANSION S29GL512P10 datasheet:
  https://www.cypress.com/file/219926/download

- Indirect Programming of BPI PROMs with Virtex-5 FPGAs:
  https://www.xilinx.com/support/documentation/application_notes/xapp973.pdf

3) Board has few simple peripherals onboard. 8 yellow LEDs, 8 DIP switches, active-low push button, 16 ohm passive speaker. Board is equipped with 50 MHz CMOS crystal oscillator, and two LVPECL oscillators, 75MHz and 125MHz connected to MGT tile. You can use DCM to divide or multiply clock frequency. Additional clock signals can be connected from outside.
XKF5 module has Infineon HYB39S256800DT-7 256Mbit SDRAM with maximum frequency of 143MHz, K9WAG08U1B 16Gbit NAND FLASH memory and AT24C1024 1024Kbit EEPROM. All these peripherals can be tested when VHDL demo project is loaded to FPGA. VHDL demo project includes “reprogramming mode”. In this mode, NAND and EEPROM can be reprogrammed. To program AT24C1024, connect external programmer to J19. To restore EEPROM factory settings, use “xkf5_a.bin”. To program K9WAG08U1B, connect external programmer to J20. J19 and J20 connectors also can be used to connect logic analyzer, to debug your projects.
XKF5 FPGA kit has FTDI FT2232C USB controller onboard. This controller can be used for programming onboard FPGA, or external JTAG device. Also, it can be used for communication with FPGA in UART, FIFO or MPSSE modes. To program FPGA, connect J7 to J16 and J2 to J3 with jumpers. Connect 12V to J4. Connect XKF5 kit to USB port, and install FT2232C drivers, what can be downloaded from FTDI website, if your PC doesn’t install them automatically. Program “XC3SPROG” can be used for programming XKF5 kit.
1) Download latest version of xc3sprog from http://sourceforge.net/projects/xc3sprog/
2) Place xc3sprog.exe to the folder of your ISE project, where .bit file is located.
3) Create shortcut: "C:\...\xc3sprog.exe -c ftdi -v -p 1 FILE_NAME.bit" to program XKF5 FPGA. If you want to explore more options, start "xc3sprog" from CMD. To program external JTAG device, with XKF5 onboard USB programmer, remove jumpers from J2 and J3, connect external device to J2. Programmer can work with Vref from 1.65v to 5.5v. This includes 1.8v, 2.5v, 3.3v and 5v standard signal levels. If you wish to program XKF5 kit with external programming cable, you can connect it to J3. To use all FT2232C ports for communication with FPGA, connect J7 to J15 with jumpers. Configure FT2232C, accordingly to your needs, with program “FT_PROG”. To restore factory settings, use file “FT.xml”. By default, PORT B of FT2232C is configured as UART interface and PORT A as JTAG. XKF5 board has VGA port with resistor ladder DAC. Each color signal is separated to 3 IO pins with resistors. This scheme imitates the digital to analog converter. It can be used to gain more colors on the picture. Virtex-5 FPGA System Monitor is enabled on this board. Auxiliary analog input is connected to J32.

- FT2232C datasheet:
  http://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT2232C.pdf

- FTDI's program "FT prog":
  http://www.ftdichip.com/Support/Utilities/FT_Prog_v2.8.2.0.zip

- More info about XC3SPROG:
  http://xc3sprog.sourceforge.net/

- K9WAG08U1B datasheet :
  http://datasheet.octopart.com/K9K8G08U0B-PCB0000-Samsung-datasheet-11629949.pdf

- AT24C1024 datasheet :
  http://www.atmel.com/Images/doc1471.pdf

- HYB39S256800DT-7 datasheet:
  https://pldkit.com/download/HYB39S256800.pdf

- LogiCORE IP Multi-Port Memory Controller:
  http://www.xilinx.com/support/documentation/ip_documentation/mpmc/v6_05_a/mpmc.pdf

- Virtex-5 FPGA System Monitor:
  https://www.xilinx.com/support/documentation/user_guides/ug192.pdf

4) Board has 4 GTP_DUAL tiles routed, what gives 8 GTP RocketIO Transceivers. There is 75MHz LVPECL oscillator connected to MGT_112 tile and 125Mhz oscillator connected to MGT_118. Any of onboard transceivers can be clocked from these oscillators. Transceivers also can be clocked from FPGA I/O clock. J24, J26 and J31 are SATA HOST ports. Peripherals like SATA hard drive, can be connected there. J23, J25 and J30 are SATA TARGET ports. External SATA controller can be connected there, and XKF5 will act as SATA peripheral. You can still use TARGET port as HOST, or HOST port as TARGET, if you use SATA crossover cable, instead of ordinary. There are two SMA connectors and two SATA ports, connected to MGT_116 tile. External differential clock signal can be connected to J6 and J22. Both transceivers of MGT_114, including MGTREFCLK pins, are routed to J27, 1.27mm pitch male connector. J27 also has GND and VCC 3.3V pins. Additional modules, like Ethernet PHY can be connected, and powered, from J27. When demo design is loaded to FPGA, transceivers can be tested, by looping one to another. Demo design includes Chipscope core. To use it, load design, and connect to FPGA with Chipscope Pro Analyzer 14.1.

- Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug194.pdf
- Virtex-5 FPGA RocketIO GTP Transceiver User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug196.pdf
- LogiCORE IP Virtex-5 FPGA RocketIO GTP Transceiver Wizard v2.1:
  http://www.xilinx.com/support/documentation/ip_documentation/v5_gtpwizard_ds590.pdf
- LogiCORE™ IP Virtex®-5 FPGA RocketIO™ GTP Transceiver Wizard v2.1 Getting Started Guide:
  http://www.xilinx.com/support/documentation/ip_documentation/v5_gtpwizard_gsg188.pdf
- Serial ATA Physical Link Initialization with the GTP Transceiver of Virtex-5 LXT FPGAs:
  http://www.xilinx.com/support/documentation/application_notes/xapp870.pdf

5) As described in chapter 3, of this guide, XKF5 kit can be programmed by onboard USB programmer or by external JTAG programmer. J21 is for selecting FPGA mode.
Here are jumper combinations that are valid for XKF5 board:

- Master BPI-Up mode (M[2:0] = <0:1:0>). In this mode, FPGA is loading configuration from the flash.

- JTAG mode (M[2:0] = <1:0:1>). In this mode FPGA is waiting configuration from JTAG, not loading from the flash.

Red button B1 is connected to FPGA PROGRAM_B signal. When it is pressed – FPGA is forced to start reconfiguration process. PROGRAM_B also can be pulled low by U5, MAX809TEUR voltage monitor. The function of the MAX809 is to monitor the 3.3v VCC supply voltage, and assert a PROGRAM_B signal low whenever this voltage declines below the 3.08v reset threshold. This board also has J17 connector, what is connected in parallel to B1. J17 can be used to reset the FPGA module externally. To reset module externally, connect "NO" relay contacts to J17. D10 is FPGA DONE LED. It turns on, after FPGA has finished configuration process. To configure or reconfigure FPGA from FLASH, set J21 jumpers to Master BPI-Up mode, and press B1. To clear FPGA configuration and put it in JTAG mode – set J21 jumpers to JTAG mode, and press B1. D11 is flash busy LED. When it is on, flash is performing erase or write operation.

- MAX809 datasheet:
  http://datasheets.maximintegrated.com/en/ds/MAX803-MAX810Z.pdf
- Virtex-5 FPGA Configuration User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug191.pdf

6) Board has powerful power supply, to serve the needs of VIRTEX-5 FPGA. Core voltage for FPGA is provided by ATS030A0X3-SRPH. Together with 1320uF tantalum capacitors, it is very stable, accurate, and powerful solution. ATS030A0X3-SRPH can deliver up to 30A current for FPGA core. 3.3V supply is built with PTH12050W, a highly efficient DC-DC converter. Maximum continuous output current from PTH12050W is 6A. Output 3.3V is used by board peripherals, and by FPGA

IO banks. 5V and 2.5V supplies are built with 1.5A LDO regulators and 1.2V supply is built with 3A LDO regulator. 2.5V is used for FPGA VCCAUX. 1.2V supply is used for FPGA GTP transceivers. 5V supply is needed for USB controller. Board has J18 connector - AUX I/O voltage input. Input voltage range is 1.14V-3.45V. If voltage, what is above the maximum limit is applied to J18, FPGA IC will be permanently damaged. Supply voltage for banks 3,6,13,21,23,25,26 can be selected between 3.3V and J18 VCC AUX, with J8 jumper. If some of these banks will have huge load, it is recommended to replace jumpers with solder bridge, to achieve better current flow.
J4 jack is used to connect DC power adapter. Please be careful with voltage polarity. External power supply voltage must be within range of 11V to 13V, and capable to provide at least 1A current, to test all functions with the demo design. Much bigger current may be required, for your custom FPGA design. D9 is a POWER-ON LED, with red color. When it is on, it means that input voltage is connected with correct polarity.

7) There are total 138 I/O pins, that are routed to the connectors, and can be used in your design. Please refer to the board schematics, to get information about connections. All these I/O are independent and not crossing with any module peripherals. J9 and J10 are 65-pin male arrays. I/O voltage for J9 and J10 connectors can be selected between 3.3V and J18 VCC AUX, with J8 jumper. Caution: J8 jumper can be removed only when board is turned OFF. J11 and J12 are power connectors, corresponding to banks 3,6,13,21,23,25,26. J13 and J14 are GND connectors. J5 is 6x2 female connector. It has 8 IO, 2 VCC 3.3V and 2 GND. This female connector is designed specially to support peripheral modules. Peripheral modules, with compatible male connectors, can be ordered from PLDkit web site, or from some other suppliers. Please note that you must use I/O standard “LVCMOS33” or “LVTTL” when IO voltage is set to 3.3V. Please note that HSWAPEN FPGA pin is connected to GND, this means that when FPGA is not configured, all IO pull-up resistors are enabled. When demo design is loaded to FPGA, IO connectors can be tested. Use fly wire, to connect IO pins one by one to BANK VCC. Test is passed if LEDs were turning on, every time when one of IO pins is connected to VCC. If there is missing contact, or short circuit between several IO, then LEDs will not turn on. Be careful, and don’t make a short circuit between VCC and GND. Also don’t connect 5V or 12V voltage to IO pins. J19 is I²C header, connected in parallel to boards I²C bus. J19 can be used to reprogram EEPROM, or to connect logic analyzer. J20 is NAND FLASH header, connected in parallel to NAND FLASH. J20 can be used to reprogram NAND FLASH, or to connect logic analyzer. All connectors have 2.54mm pitch. With some designs, FPGA can heat quite fast. Adhesive heatsink can be mounted on top of FPGA.

- Peripheral modules:
  https://pldkit.com/peripheral-modules

8) Board size is quite small – 100mm x 100mm.
It can be mounted inside of some other device.
Every corner of the PCB has metalized 3.1MM mounting hole, connected to GND. You can use M3 bolts and spacers, to fasten XKF5 on some surface.

Powering up the board for the first time

1) Connect 12V 1A to J4, with correct polarity.
2) Demo design will be automatically loaded into FPGA from the flash.
3) LEDs D1-D8 will start blinking. Red power LED and green DONE LED must be constantly ON.
4) Connect XKF5 to your computer with micro-USB cable. Install drivers. Establish UART terminal connection with settings 115200-8-n-1.
5) XKF5 will send welcome note to UART, if any key, except “1” - “9” is pressed.
6) If button “1” is pressed, XKF5 will enter to FTDI test mode. In this mode, FTDI connections to FPGA can be tested. To perform this test, connect J7 to J15 with jumpers. Download FTDI test utility from here: http://www.ftdichip.com/Support/Utilities/FT2232H_UART.rar
Unzip it, close UART terminal, and start “FT2232_UART.exe” from folder “\FT2232H_UART\bin\Release”. Tick options “program EEPROM” and “Check RI/DCD pins”. Press button “start”. Now, EEPROM is reprogrammed. Unplug USB and plug again. Wait until driver is installed. Untick “program EEPROM” and tick “Repeat Test”. Press button “start”. Test should fail, if DIP switch 1 or 2 is ON. Otherwise, if everything is done correctly, test must pass.

XKF5 enters FTDI test mode for 5 minutes, so, if it is returned to normal mode, while you were preparing, enter again. When testing is finished, connect J7 to J16 with jumpers.
Use program "FT_PROG" and file “FT.xml", to restore XKF5 93c46 EEPROM factory settings.
7) If button “2” is pressed, XKF5 will enter reprogramming mode. In this mode, AT24C1024 EEPROM and K9WAG08U1B NAND FLASH can be reprogrammed.
8) If button “3” is pressed, XKF5 will enter IO/DIP test mode. S1, S2, J10, J9 and J5 can be tested. Turn on DIP switches one by one or connect IO pins to VCC 3.3V one by one. If one IO pin is connected to VCC, or one DIP is ON - all LEDs will turn ON. If none or several pins connected at the same time - LEDs will stay OFF. When LEDs turn on, beep sound is produced.
9) If button “4” is pressed, XKF5 will perform a speaker test. Melody can be changed with DIP switches.
10) If button “5” is pressed, XKF5 will perform NAND FLASH test. XKF5 will read full identification of NAND chip, compare it to preset values, and report “PASSED”, if they are matched.
11) If button “6” is pressed, MicroBlaze will execute the RAM test.
12) Press “7” to enter GTP transceivers test mode. Current consumption and heat dissipation of the board will increase when you will enter this mode. Follow the onscreen instructions to perform the test. System will switch back to main menu after 10 minutes, or if BTN2 or BTN1 is pressed.
13) Press “8” to enter VGA test mode. VGA demo will be generated. VGA I^2C data will be read and sent to UART.
14) Press “9” to test multiboot feature of VIRTEX-5 FPGA. Follow the onscreen instructions to perform the test.

Model name chart

XKF5-110-512-256-16 Rev. A

PLD Manufacturer
X = Xilinx

Board Type
K = Kit

PLD Type
F = FPGA

PLD Family
5 = VIRTEX-5

PLD SIZE
110 = VLX110T

Configuration FLASH size
512 = 512Mbit

RAM size
256 = 256Mbit

NAND FLASH size
16 = 16Gbit

Board revision
Rev. A = Revision A