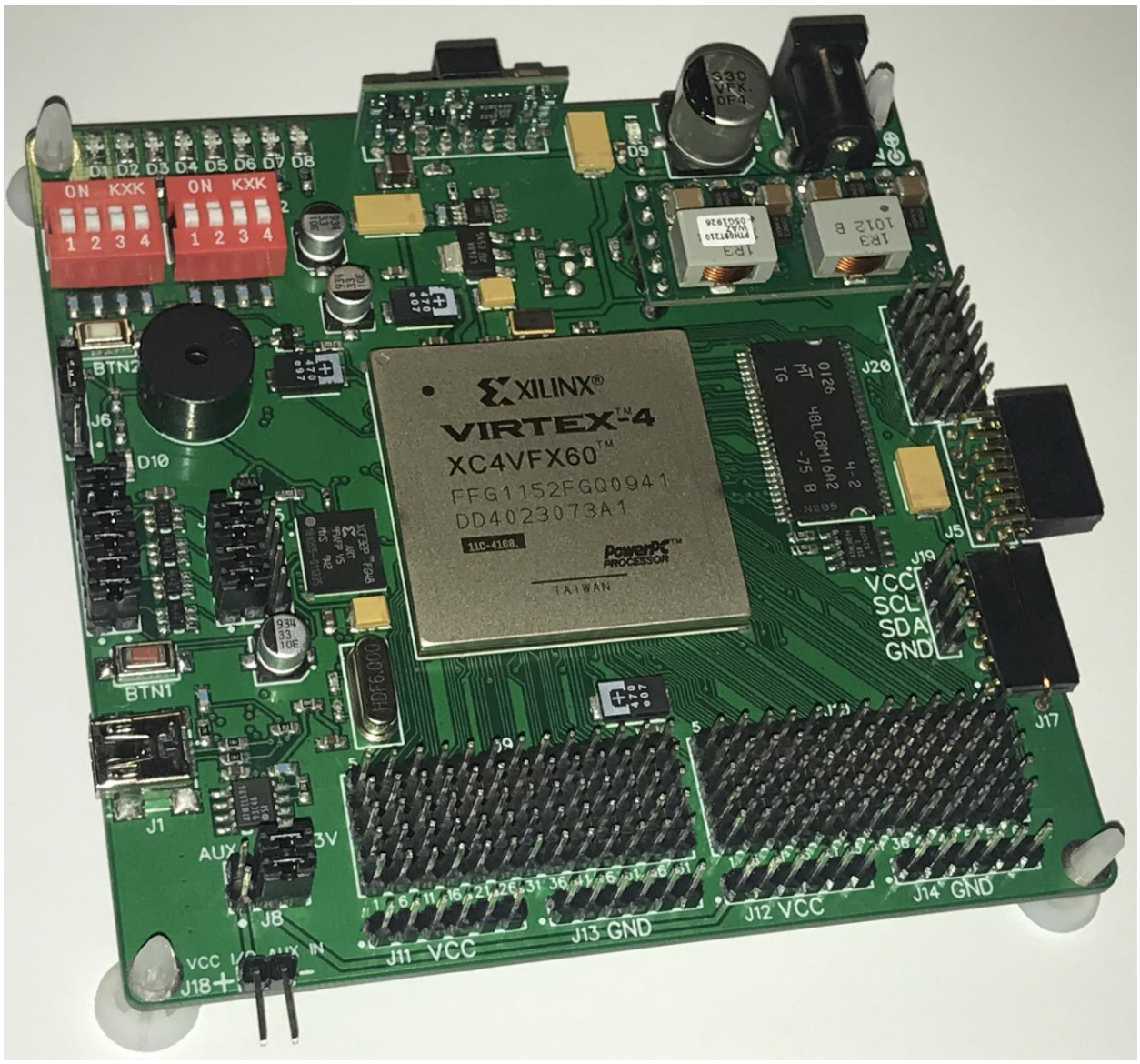
XILINX VIRTEX-4 FPGA KIT USER's GUIDE

MODEL: XKF4-60-32-128-16 Revision B



Introduction

Xilinx Virtex-4 XKF4 FPGA kit is a low cost, powerful and easy to use tool. Designed for rapid prototyping and implementing FPGA designs. Kit can be used for educational purposes. Kit can work independently, or as control module in the bigger design.

Features

1) XILINX XC4VFX60 FPGA
- 56880 Logic Cells
- 128 XtremeDSP Slices
- 232x 18Kb RAM blocks (4176Kb, 500MHz)
- 12 Digital Clock Managers
- 4 Ethernet MACs
- 2 PowerPC Processor Blocks
- 576 User I/O (251 routed on this board)

2) XILINX XCF32P FLASH
- 32Mbit Platform Flash PROM
- IEEE Standard 1149.1/1532 Boundary-Scan (JTAG) support for programming
- Endurance of 20000 Program/Erase Cycles

3) FTDI FT2232C USB controller
- Can be used as onboard USB JTAG programmer
- Can be used for communication in UART/FIFO/MPSSE modes
- Buffered port for programming external JTAG devices. Vref 1.65V -5.5V

4) Onboard IO peripherals
- 100MHz CMOS oscillator
- 8 LEDs
- 8 DIP switches
- Speaker
- 1 push button
- 128Mbit 133MHz SDRAM
- 16Gbit NAND FLASH
- 1024Kbit EEPROM

5) Handy configuration
- Configuration from onboard USB programmer
- Configuration from external programmer
- Mode select jumper (JTAG or FLASH)
- DONE LED
- Push button for manual initiation of configuration process
- Reset supervision by voltage monitor

6) Onboard power supply
- 3.3V 8A (IO, PERIPHERALS)
- 2.5V 1.5A (VCCAUX)
- 1.2V 30A (CORE VOLTAGE)
- 5V 1.5A (USB controller)
- 1.8V 1A (Platform FLASH)
- Input voltage range 11V – 13V
- POWER-ON LED

- AUX input for I/O voltage 1.14V-3.45V

7) 142 independent I/O routed to the connectors + additional outputs
- Two 5x13 male pin arrays (130 IO) with selectable IO voltage
- One 2x6 female connector (8 IO, 2 GND, 2 VCC 3.3V)
- One 1x6 female connector (4 IO, 1 GND, 1 VCC 3.3V)
- Peripheral modules support
- 2.54mm pitch for all connectors
- I²C header
- NAND FLASH header
- Test points for FPGA temperature diode

8) Small 100x100mm PCB with M3 mounting holes.

Instructions

1) Combining Advanced Silicon Modular Block (ASMBL™) architecture with a wide variety of flexible features, the Virtex®-4 family from Xilinx greatly enhances programmable logic design capabilities, making it a powerful alternative to ASIC technology. This board has XC4VFX60 FF1152 11C FPGA (1152 ball package, speed grade 11, commercial temperature range 0°C to +85°C)

- Virtex-4 Family Overview:
  http://www.xilinx.com/support/documentation/data_sheets/ds112.pdf
- Virtex-4 FPGA DC and Switching Characteristics:
  http://www.xilinx.com/support/documentation/data_sheets/ds302.pdf
- Virtex-4 FPGA User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug070.pdf
- Virtex-4 FPGA Configuration User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug071.pdf
- PowerPC 405 Processor Block Reference Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug018.pdf
- XtremeDSP for Virtex-4 FPGAs User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug073.pdf

2) XILINX XCF32P is 32 Mbit platform Flash PROM with JTAG interface. Demo design will be stored to flash during manufacturing. With this demo, most of the kit functions can be tested. XCF32P is wired in parallel mode.

- Platform flash PROM user guide:
  http://www.xilinx.com/support/documentation/user_guides/ug161.pdf

3) XKF4 FPGA kit has FTDI FT2232C USB controller onboard. This controller can be used for programming onboard FPGA, FLASH or external JTAG device. Also, it can be used for communication with FPGA in UART, FIFO or MPSSE modes.
To program FPGA or FLASH, connect J7 to J16 and J2 to J3 with jumpers. Connect 12V to J4. Connect XKF4 kit to USB port, and install FT2232C drivers, what can be downloaded from FTDI website, if your PC doesn't install them automatically.
It is recommended to use program "XC3SPROG", for programming XKF4 kit.
1) Download latest version of xc3sprog from http://sourceforge.net/projects/xc3sprog/
2) Place xc3sprog.exe to the folder of your ISE project, where .bit file is located.
3) Create shortcuts on your desktop:

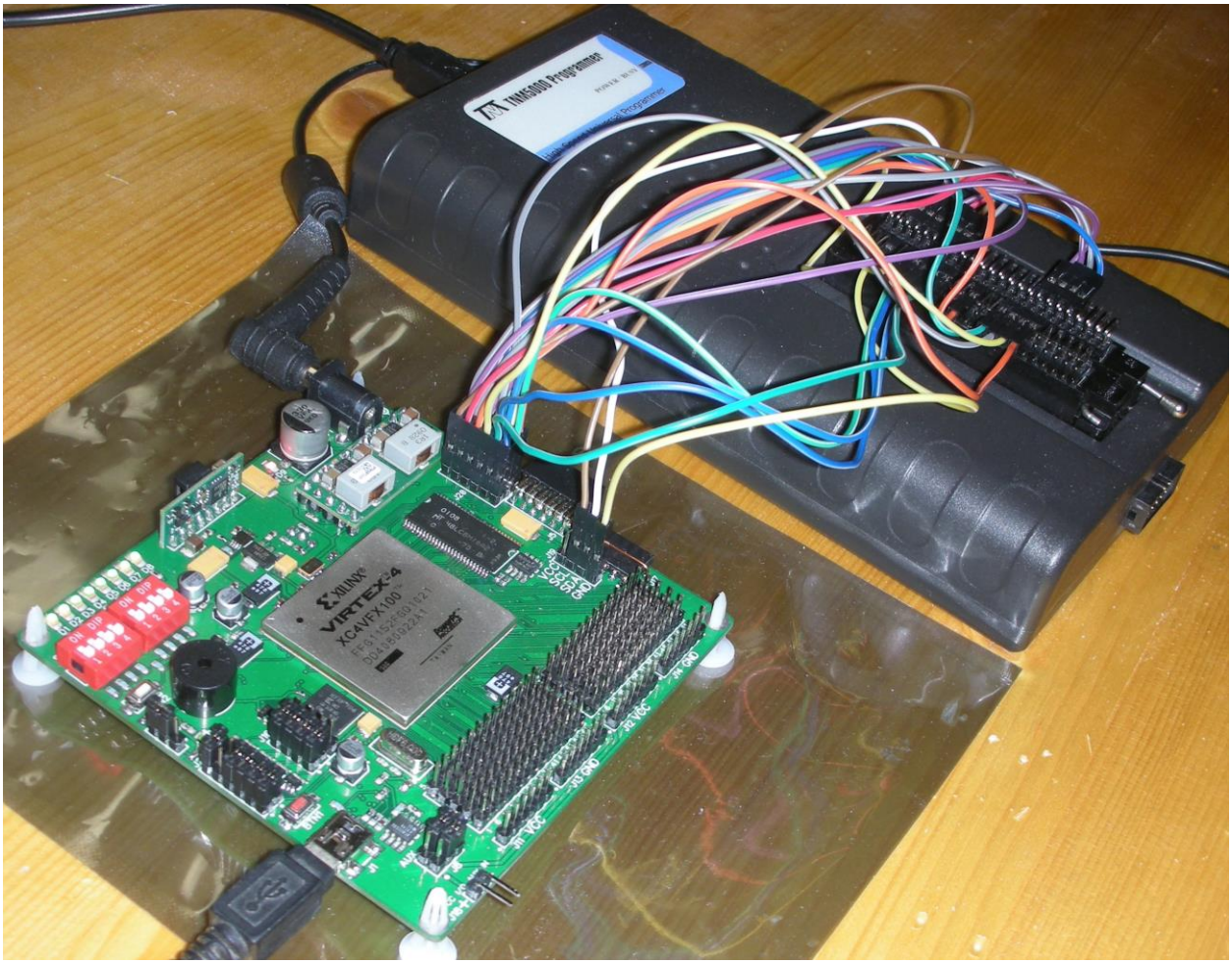
"C:\...\xc3sprog.exe -c ftdi -v -p 1 FILE_NAME.bit" to program XKF4 FPGA.
"C:\...\xc3sprog.exe -c ftdi -X parallel -R -v -p 0 FILE_NAME.bit" to program XKF4 FLASH.
4) If something went wrong, or you want to explore more options, start "xc3sprog" from CMD.

To program external JTAG device, with XKF4 onboard USB programmer, remove jumpers from J2 and J3, connect external device to J2. J2 is connected to buffer IC's. They are needed to amplify driving current and to widen the supported voltage levels. Programmer can work with Vref from 1.65v to 5.5v. This includes 1.8v, 2.5v, 3.3v and 5v standard signal levels. If you wish to program XKF4 kit with external programming cable, you can connect it to J3.
To use all FT2232C ports for communication with FPGA, connect J7 to J15 with jumpers.
Configure FT2232C, accordingly to your needs, with program "FT_PROG".
To restore factory settings, use file "FT.xml". By default, PORT B of FT2232C is configured as UART interface and PORT A as JTAG.

- FT2232C datasheet:
  http://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT2232C.pdf
- FTDI's program "FT prog":
  http://www.ftdichip.com/Support/Utilities/FT_Prog_v2.8.2.0.zip
- Drivers and more info about FT2232C:
  http://www.ftdichip.com/Products/ICs/FT2232D.htm
- More info about XC3SPROG:
  http://xc3sprog.sourceforge.net/
- XKF4 FPGA kit also can be programmed with program "urjtag":
  http://urjtag.org/

4) Board has few simple peripherals onboard: 8 yellow LEDs, 8 active-low DIP switches with pull up resistors, 16 ohm passive speaker, active-low push button with pull up resistor.
XKF4 kit is equipped with 100 MHz CMOS crystal oscillator. You can use DCM to divide or multiply clock frequency. Additional clock signals can be connected from outside.
XKF4 kit has 128Mbit 133MHz MT48LC8M16A2-75 SDRAM memory. Zip archive, for this board, includes PowerPC demo project, for testing SDRAM memory. PowerPC executes RAM tests and send results to UART. LEDs indicate DCM, reset and MPMC statuses. BTN2 resets PowerPC.
XKF4 kit has K9WAG08U1B 16Gbit NAND FLASH memory and AT24C1024 1024Kbit EEPROM. NAND flash memory and EEPROM can be tested when VHDL demo project is loaded to FPGA. VHDL demo project includes "reprogramming mode". In this mode, NAND and EEPROM can be reprogrammed. To program AT24C1024, connect external programmer to J19. To restore EEPROM factory settings, use "xkf4_b.bin". To program K9WAG08U1B, connect external programmer to J20. We recommend using "TNM5000 universal programmer" for EEPROM/NAND programming operations. Additional fly wires might be required, to connect TNM5000 to XKF4. J19 and J20 connectors also can be used to connect logic analyzer, to debug your projects.

- MT48LC8M16A2 datasheet:
  https://www.micron.com/~/media/documents/products/data-sheet/dram/128mb_x4x8x16_ait-aat_sdram.pdf
- K9WAG08U1B datasheet :
  http://datasheet.octopart.com/K9K8G08U0B-PCB0000-Samsung-datasheet-11629949.pdf
- AT24C1024 datasheet :
  http://www.atmel.com/Images/doc1471.pdf
- TNM5000 universal programmer:
  http://www.tnmelectronics.com/English/5000.html



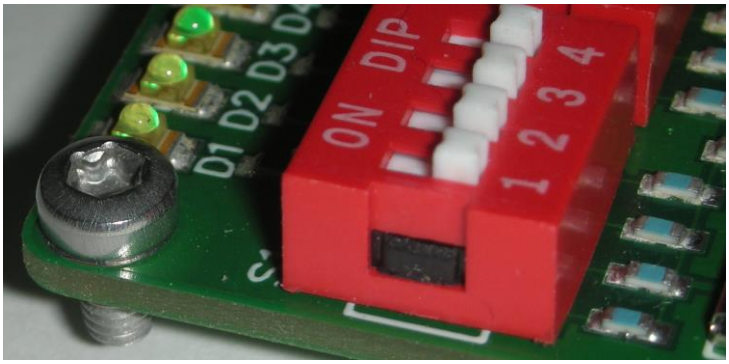
5) Red button BTN1 is connected to FPGA PROGRAM_B signal. When it is pressed – FPGA is forced to start reconfiguration process. PROGRAM_B also can be pulled low by U4, MAX809TEUR voltage monitor.
As described in chapter 3, of this guide, XKF4 kit can be programmed by onboard USB programmer or by external JTAG programmer.
D10 is FPGA DONE LED. It turns on, after FPGA has finished configuration process.
J6 is for setting FPGA mode. When jumper is in position “F”, this is Master SelectMAP mode (loading from flash). When jumper is in position “J”, this is JTAG mode (waiting configuration from JTAG, not loading from the flash).
To configure or reconfigure FPGA from FLASH, set J6 jumper to “F”, and press BTN1.
To clear FPGA configuration and put it in JTAG mode – set J6 jumper to “J”, and press BTN1.

6) Board has powerful power supply, to serve the needs of VIRTEX-4 FPGA. Core voltage for FPGA is provided by PTH08T210W. Together with 2350uF tantalum capacitors and TurboTrans™ Technology, it is very stable, accurate and powerful solution. PTH08T210W can deliver up to 30A current for FPGA core.
3.3V supply is built with 8A DC-DC converter, PTV12010W. 3.3V is used by board peripherals and by FPGA IO banks.
Board has J18 connector, AUX I/O voltage input. Input voltage range is 1.14V-3.45V. If voltage, above the maximum limit is applied to J18, FPGA IC will be permanently damaged.
Supply voltage for banks 4,8,12,7,11 can be selected between 3.3V and VCC AUX, with J8 jumpers. If some of these banks will have huge load, it is recommended to replace jumpers with

solder bridges, to achieve better current flow.
2.5V supply, what is used for FPGA VCCAUX, is built with 1.5A LDO.
There is voltage regulator, to produce 5V for powering USB controller.
Another, voltage regulator, converts 5V to 1.8V for XCF32P core voltage.
J4 input power voltage must be within range of 11V to 13V. There must be at least 0.5A current, to start the board with demo design. Much bigger current may be required, for your custom FPGA design. Use J4 DC jack to connect DC power adapter. Be careful with voltage polarity, positive "inside", negative "outside".
D9 is a POWER-ON LED, with red color. When it is on, it means that there is input DC voltage connected.

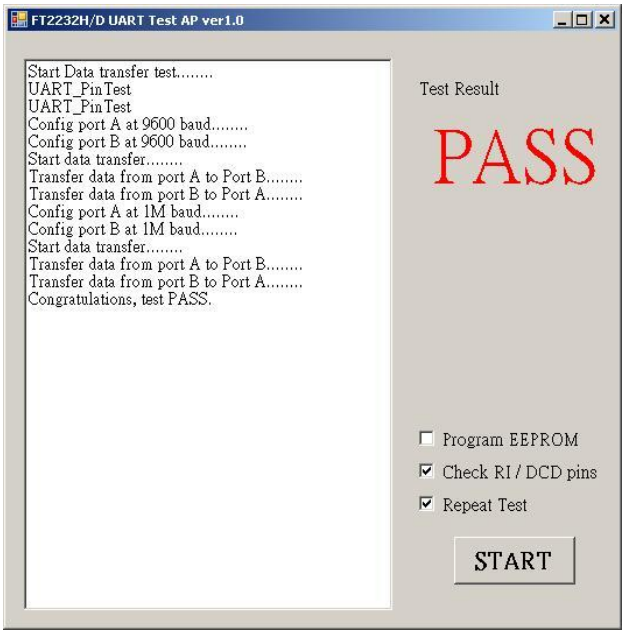
7) There are total 142 independent I/O pins, what are routed to the connectors, and can be used in your design. Please refer to the board schematics, to get information about connections. These I/O are not crossing with any module peripherals. J9 and J10 are 65-pin male arrays. J9 is routed to BANK4, BANK8 and BANK12. J10 is routed to BANK7 and BANK11. Voltage for banks 4, 8 and 12 can be set to 3.3V by connecting J8 pin6 to J8 pin4, to VCC AUX by connecting J8 pin2 to J8 pin4. Voltage for banks 7 and 11 can be set to 3.3V by connecting J8 pin5 to J8 pin3, to VCC AUX by connecting J8 pin1 to J8 pin3. Caution: J8 jumpers can be removed only when board is turned OFF. J11 and J13 are power connectors, corresponding to banks 4, 8, 12 and connector J9.
J12 and J14 are power connectors, corresponding to banks 7, 11, and connector J10.
J5 is 6x2 female connector. It has 8 IO, 2 VCC 3.3V and 2 GND. J17 is 6x1 female connector. It has 4 IO, 1 VCC 3.3V and 1 GND. These female connectors are designed specially to support peripheral modules. Peripheral modules, with compatible male connectors, can be ordered from PLDkit web site, or from some other suppliers.
Please note that you must use I/O standard "LVCMOS33" or "LVTTL", when IO voltage is 3.3V.
Please note that HSWAPEN FPGA pin is connected to GND, this means that when FPGA is not configured, all IO pull-up resistors are enabled.
When demo design is loaded to FPGA, IO connectors can be tested. Use fly wire, to connect IO pins one by one to BANK VCC. Test is passed, if LEDs are turning on, every time when one of IO pins is connected to VCC. If there is missing contact or short circuit between IO, LEDs will not turn on. Be careful, and don't make short circuit between VCC and GND.
J19 is I^2C header, connected in parallel to boards I^2C bus. J19 can be used to reprogram EEPROM, or to connect logic analyzer.
J20 is NAND FLASH header, connected in parallel to NAND FLASH. J20 can be used to reprogram NAND FLASH, or to connect logic analyzer.
All connectors have 2.54mm pitch.
Internal FPGA thermal diode is routed to test points TP2 (TDP_0) and TP1 (TDN_0).
By connecting this diode to an external signal conditioning IC (thermal monitor), the die temperature could be determined. With some designs, FPGA can heat quite fast. Adhesive heatsink can be mounted on top of FPGA.

8) Board size is quite small – 100mm x 100mm. It can be mounted inside of some other device.
Every corner of the PCB has metalized 3.1MM mounting hole, connected to GND.
You can use M3 bolts and spacers, to fasten XKF4 on some surface.



Powering up the board for the first time

1) Connect 12V 1A to J4, with correct polarity.
2) Demo design will be automatically loaded into FPGA from the flash, if jumper J6 is in position “F”.
3) LEDs D1-D8 will start blinking. Red power LED and green DONE LED must be constantly ON.
4) Connect XKF4 to your computer with mini-USB cable. Install drivers. Establish UART terminal connection with settings 115200-8-n-1.
5) XKF4 will send welcome note to UART, if any key, except “1”,”2”,”3”,“4”,“5” or “6” is pressed.
6) If button “1” is pressed, XKF4 will enter to FTDI test mode. In this mode, FTDI connections to FPGA can be tested. To perform this test, connect J7 to J15 with jumpers. Download FTDI test utility from here: http://www.ftdichip.com/Support/Utilities/FT2232H_UART.rar
Unzip it, close UART terminal, and start “FT2232_UART.exe” from folder “\FT2232H_UART\bin\Release”. Tick options “program EEPROM” and “Check RI/DCD pins”. Press button “start”. Now, EEPROM is reprogrammed. Unplug USB, and plug again. Wait until driver is installed. Untick “program EEPROM” and tick “Repeat Test”. Press button “start”. Test should fail, if DIP switch 1 or 2 is ON. Otherwise, if everything is done correctly, test must pass.



XKF4 enters FTDI test mode for 5 minutes, so, if it is returned to normal mode, while you were preparing, enter again. When testing is finished, connect J7 to J16 with jumpers.
Use program "FT_PROG" and file “FT.xml", to restore XKF4 93c46 EEPROM factory settings.

7) If button “2” is pressed, XKF4 will enter reprogramming mode. In this mode, AT24C1024 EEPROM and K9WAG08U1B NAND FLASH can be reprogrammed.
More details about this on pages 4-5, of this guide.
8) If button “3” is pressed, XKF4 will enter IO/DIP test mode. S1, S2, J10, J9, J5 and J17 can be tested. Turn on DIP switches one by one or connect IO pins to VCC 3.3V one by one. If one IO pin is connected to VCC, or one DIP is ON - all LEDs will turn ON. If none or several pins connected at the same time - LEDs will stay OFF. When LEDs turn on, beep sound is produced.
9) If button “4” is pressed, XKF4 will perform quick speaker test.
10) If button “5” is pressed, XKF4 will perform NAND FLASH test. XKF4 will read full identification of NAND chip, compare it to preset values, and report “PASSED”, if they are matched.
11) If button “6” is pressed, PowerPC will execute the RAM test.

Model name chart