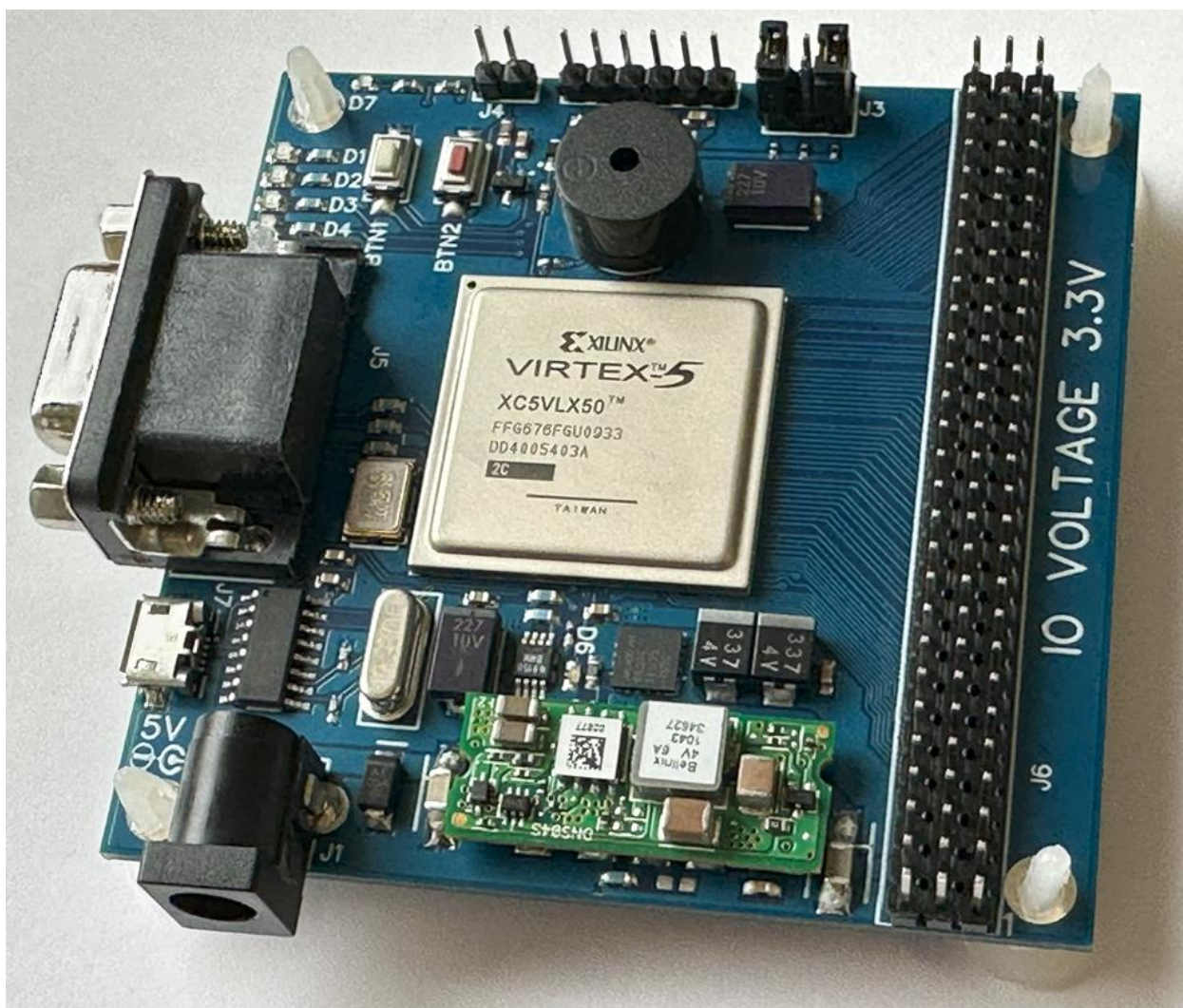


# XILINX VIRTEX-5 FPGA KIT USER's GUIDE

**MODEL: XK2F5-64 Revision A**



# Introduction

The Xilinx Virtex-5 XK2F5 FPGA kit is designed for rapid prototyping and FPGA design implementation. The board is suitable for educational purposes and can operate as a standalone unit or as a control module within a larger system.

## Features

- 1) XILINX XC5VLX50 FFG676 2C FPGA
  - 7200 Virtex-5 Slices (46080 Logic Cells)
  - 48 DSP48E Slices
  - 48x 36Kb RAM blocks (1728Kb, 550MHz)
  - 6 Clock Management Tiles
  - 440 User I/O (135 routed on this board)
- 2) INTEL JS28F640J3 FLASH
  - 64Mbit
  - BPI Interface
  - FPGA configuration
  - Post-configuration access
  - 100,000 erase cycles per block
- 3) Onboard IO peripherals
  - CH340G USB UART port
  - 50MHz CMOS oscillator
  - 4 IO LEDs
  - IO push button
  - Speaker
  - VGA port
- 4) Handy configuration
  - Standard 2.54mm JTAG header
  - Mode select jumpers
  - DONE LED
  - Push button for manual initiation of configuration process
  - Header for external reset
  - Reset supervision by voltage monitor
- 5) Onboard power supply
  - 3.3V 6A (IO, PERIPHERALS)
  - 2.5V 1.5A (VCCAUX)
  - 1V 4A (CORE VOLTAGE)
  - Input voltage range 4.5V – 5.5V
  - POWER-GOOD LED
- 6) 81 independent I/O routed to the connector
  - J6 3x29 male pin connector (81 IO, 3 VCC, 3 GND)
  - 2.54mm pitch
  - 3.3V I/O voltage
  - Small 74x75mm PCB

## Instructions

- 1) The Virtex-5 family provides the newest most powerful features in the FPGA market. In addition to the most advanced, high-performance logic fabric, Virtex-5 FPGAs contain many hard-IP system level blocks. These features allow advanced logic designers to build the highest levels of performance and functionality into their FPGA-based systems. Built on a 65-nm state-of-the-art copper process technology, Virtex-5 FPGAs are a programmable alternative to custom ASIC technology. This board has XC5VLX50 FFG676 2C FPGA (676 ball package, speed grade 2, commercial temperature range 0°C to +85°C).
  - Virtex-5 Family Overview:  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds100.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf)
  - Virtex-5 FPGA DC and Switching Characteristics:  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds202.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf)
  - Virtex-5 FPGA User Guide:  
[http://www.xilinx.com/support/documentation/user\\_guides/ug190.pdf](http://www.xilinx.com/support/documentation/user_guides/ug190.pdf)
  - Virtex-5 FPGA XtremeDSP Design Considerations:  
[http://www.xilinx.com/support/documentation/user\\_guides/ug193.pdf](http://www.xilinx.com/support/documentation/user_guides/ug193.pdf)
- 2) INTEL JS28F640J3 is 64 Mbit NOR Flash with 0.13  $\mu\text{m}$  ETOX™ VIII process technology. A demo design will be preloaded into the flash during manufacturing. This demo allows for testing the board's functionality. Flash is wired in parallel mode, following iMPACT configuration should be used:

**PROM File Formatter**

**Step 1. Select Storage Target**

Storage Device Type :

- Xilinx Flash/PROM
  - Non-Volatile FPGA
    - Spartan3AN
  - SPI Flash
    - Configure Single FPGA
    - Configure MultiBoot FPGA
  - BPI Flash
    - Configure Single FPGA
    - Configure MultiBoot FPGA
    - Configure from Paralleled PROMs
  - Generic Parallel PROM

**Step 2. Add Storage Device(s)**

Target FPGA: Virtex5

Storage Device (Bytes): 8M

Add Storage Device Remove Storage Device

8M

**Step 3. Enter Data**

General File Detail		Value
Checksum Fill Value	FF	
Output File Name	Untitled	
Output File Location	C:\Xilinx\Projects\completed\WK2	

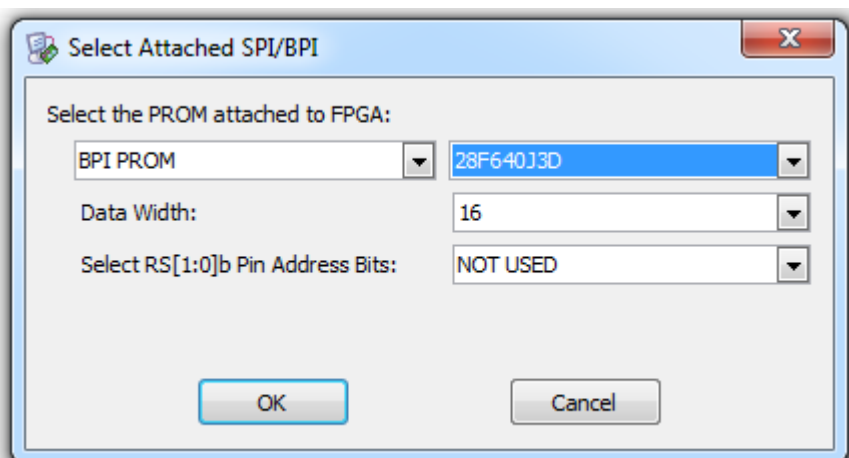
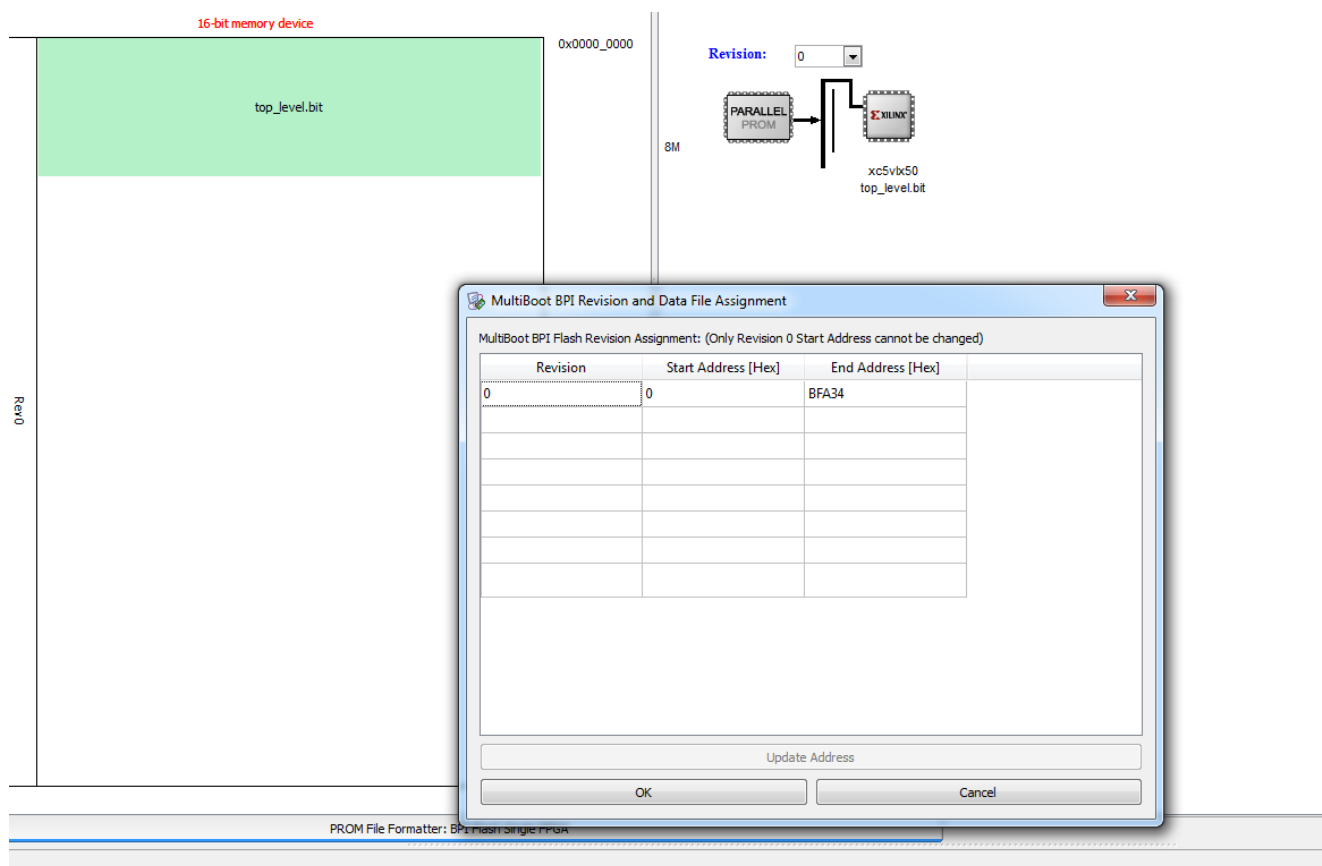
Flash/PROM File Property		Value
File Format	MCS	
Data Width	x16	
Add Non-Configuration Data Files	No	

**Description:**

In this step, you will enter information to assist in setting up and generating a PROM file for the targeted storage device and mode.

- **Checksum Fill Value:** When data is insufficient to fill the entire memory of a PROM, the value specified here is used to calculate the checksum of the unused portions.
- **Output File Name:** This allows you to specify the base name of the file to which your PROM data will be written
- **Output File Location:** This allows you to specify the directory in which the file named above will be created
- **File Format:** PROM files can be generated in any number of industry standard formats. Depending on the PROM file format your PROM programmer uses, you output a MCS

OK Cancel Help



- INTEL JS28F640J3 datasheet:  
<https://www.pldkit.com/download/28F128J3D75.pdf>
  - Indirect Programming of BPI PROMs with Virtex-5 FPGAs:  
[https://www.xilinx.com/support/documentation/application\\_notes/xapp973.pdf](https://www.xilinx.com/support/documentation/application_notes/xapp973.pdf)
- 3) The board includes a few simple onboard peripherals: four yellow LEDs, an active-low push button, and a 16-ohm passive speaker. It is equipped with a 50 MHz CMOS crystal oscillator, and a Digital Clock Manager (DCM) can be used to divide or multiply the clock frequency. Additional clock signals can also be connected externally. The board features a CH340G USB UART port and a basic VGA output, with R, G, B, HS, and VS signals connected directly to the FPGA.

All peripherals can be tested by loading a VHDL demo project onto the FPGA. The Virtex-5 FPGA System Monitor is also enabled on this board.

- Virtex-5 FPGA System Monitor:  
[https://www.xilinx.com/support/documentation/user\\_guides/ug192.pdf](https://www.xilinx.com/support/documentation/user_guides/ug192.pdf)
- 4) The XK2F5 FPGA kit can be programmed via the J2 JTAG header using an external JTAG programmer. The red button, BTN2, is connected to the FPGA's PROGRAM\_B signal. When BTN2 is pressed, the FPGA is forced to start the reconfiguration process. The PROGRAM\_B signal can also be pulled low by the U6 MAX809TEUR voltage monitor.  
The board features a J4 connector, which is connected in parallel with BTN2. J4 allows external resetting of the FPGA board—this can be done by connecting the “NO” (Normally Open) relay contacts to J4.  
LED D7 serves as the FPGA DONE indicator. It lights up once the FPGA has completed its configuration process.  
The J3 header is used to set the FPGA configuration mode:
  - M0 and M2 jumpers inserted: Master BPI-Up mode (configuration is loaded from flash memory).
  - Only M1 jumper inserted: JTAG mode (FPGA waits for configuration from a JTAG programmer and does not load from flash).

To configure or reconfigure the FPGA from flash, set the J3 jumpers to Master BPI-Up mode and press BTN2. To clear the configuration and enter JTAG mode, set the J3 jumper to JTAG mode and press BTN2.
- Virtex-5 FPGA Configuration User Guide:  
[http://www.xilinx.com/support/documentation/user\\_guides/ug191.pdf](http://www.xilinx.com/support/documentation/user_guides/ug191.pdf)
- MAX809 datasheet:  
<http://datasheets.maximintegrated.com/en/ds/MAX803-MAX810Z.pdf>
- 5) The board features a compact power supply designed to meet the requirements of the VIRTEX-5 FPGA. A MAX8556 LDO provides the 1V core voltage at up to 4A, while a DNS04 DC-DC converter supplies the 3.3V IO voltage at up to 6A. Together with tantalum capacitors, this setup delivers a stable, accurate, and high-performance power solution.  
The 3.3V rail powers both the board's peripherals and the FPGA IO. A 2.5V supply, used for the FPGA's VCCAUX, is generated by the U2 LDO regulator, capable of delivering up to 1.5A. Input power is supplied via connector J1 and must be within the 4.5V to 5.5V range. A minimum of 1A is required to start the board with the demo design. However, custom FPGA designs may demand higher current.  
D6 is a red POWER-GOOD LED. When illuminated, it indicates that the 2.5V supply is present and the 1V regulator output is within  $\pm 10\%$  of its nominal voltage.
- Virtex-5 FPGA DC and Switching Characteristics:  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds202.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf)
- 6) There are a total of 81 independent I/O pins routed to the J6 connector, which are available for use in your design. Please refer to the board schematics for detailed connection information. These I/O lines are not shared with any on-board peripherals, ensuring full flexibility.  
The J6 connector is an 87-pin male header, consisting of: 81 I/O pins, 3 GND pins, 3 VCC pins. You must use the I/O standards LVCMOS33 or LVTTTL, as the I/O voltage is 3.3V.

The HSWAPEN FPGA pin is tied to GND. This means that, before configuration, all unused I/O pins have internal pull-up resistors enabled. When the demo design is loaded onto the FPGA, you can test the I/O connectors as follows:

Use a fly wire to connect each I/O pin, one at a time, to J6 pin 4 (IO VCC).

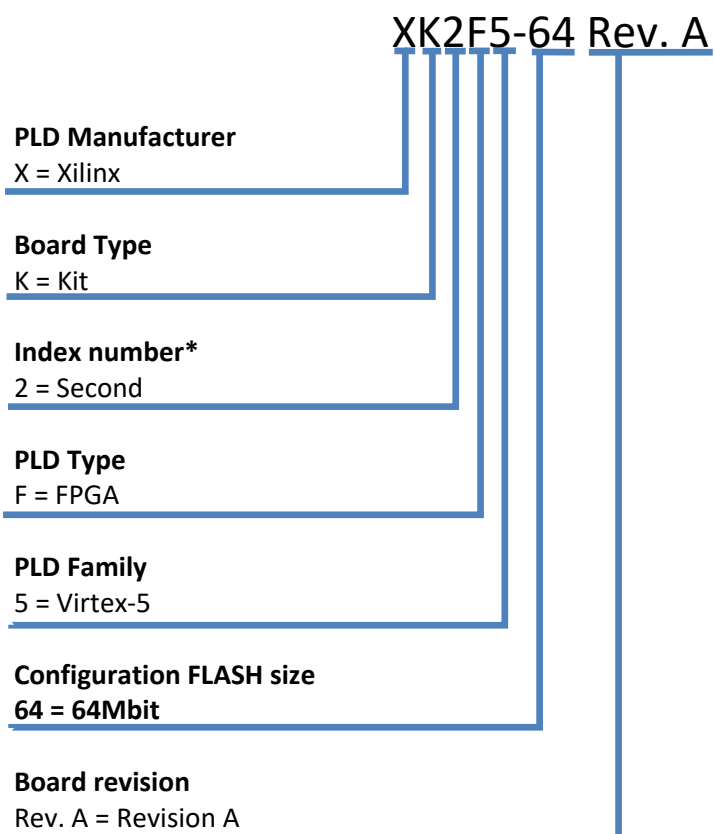
The test is successful if LEDs lights up each time an I/O pin is connected to VCC.

If a contact is missing or there is a short circuit between I/O pins, LEDs will not light up.

Be careful during testing. Do not create a short circuit between VCC and GND, as this may damage the board. All connectors on the board have a 2.54 mm pitch. The board itself is compact, with dimensions of 74 mm × 75 mm, making it suitable for integration into other devices or enclosures.

Each corner of the PCB has a metalized 3.1 mm mounting hole, which is electrically connected to GND. These holes are designed for M3 bolts and spacers, allowing the board to be securely mounted onto a surface or inside a chassis.

## Model name chart



\*Index number is used to distinguish from similar existing model