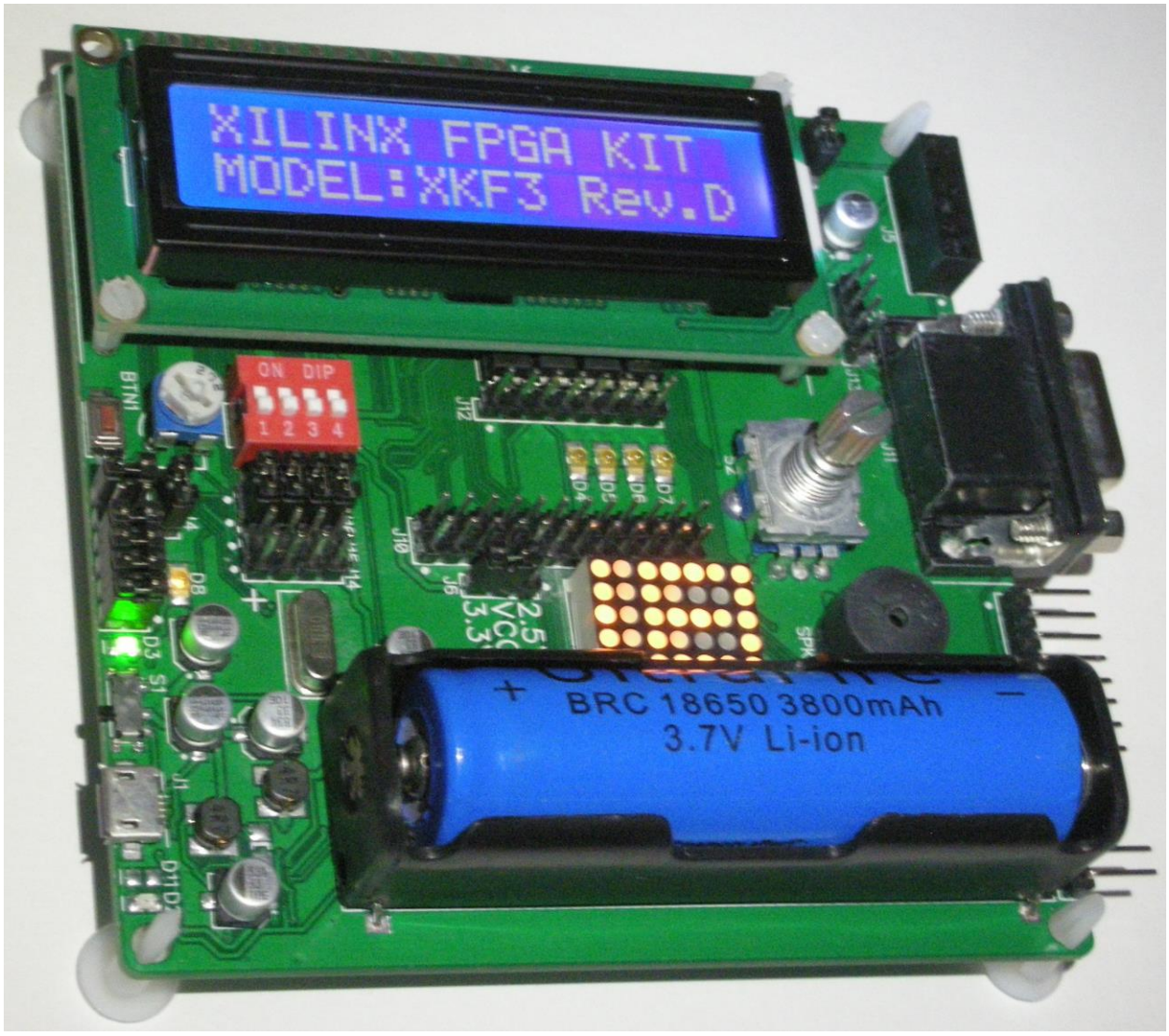
XILINX SPARTAN-3 FPGA KIT USER's GUIDE

MODEL: XKF3 Revision D



Introduction

Xilinx SPARTAN-3 XKF3 FPGA development kit is designed to study FPGA programming, or develop FPGA based projects. Also, it can be used as main control block in your machine. It includes many onboard peripherals to serve these needs. This kit doesn't require special programming cable. Onboard USB controller allows JTAG programming and UART communication. When needed, it can be used as USB programmer, for programming any other external JTAG device, not necessarily XILINX. Documentation includes easy, step by step instructions, and demo projects, for complete beginners. This kit has Li-ion battery, what can be charged from USB port or from any micro-USB wall charger.

Features

1) XILINX XC3S200 FT256 4C FPGA
- 200000 gates (4320 Logic Cells)
- 173 User I/O (127 routed on this board)
- 12x 18x18 hardware multipliers
- 12x 18K-bits block RAMs (216K)
- 4 Digital Clock Managers
- Fully supported by latest XILINX design tools

2) XILINX XCF01S VO20C FLASH
- 1 Mbit Platform Flash PROM
- IEEE Standard 1149.1/1532 Boundary-Scan (JTAG) support for programming
- Endurance of 20000 Program/Erase Cycles
- Fully supported by latest XILINX design tools

3) FTDI FT2232D USB controller
- USB to JTAG port A
- USB to UART port B
- Buffered port for programming external JTAG devices. Vref 1.65V -5.5V

4) Onboard IO peripherals
- 4 LEDs
- 4 DIP switches
- Speaker
- 50 MHz CMOS crystal oscillator
- VGA port
- 16x2 Character LCD (HD44780, or functionally equal graphics controller)
- Rotary Encoder
- 5x7 LED Matrix
- 4 optocoupled IO inputs (Full isolation mode, common GND mode, common VCC mode)
- 4 optocoupled IO outputs (Full isolation)
- AT24C256 256Kbit EEPROM
- LM75 Temperature sensor
- PCF8563 Real time clock
- ULN2003 Transistor array
- 64Mbit SDRAM

5) Handy configuration
- Configuration from onboard USB programmer
- Configuration from external programmer
- Mode select jumper (JTAG or FLASH)

- DONE LED
- Reset push button

6) Onboard power management
- Standard micro USB connector
- High capacity Li-ion battery
- Onboard charger with status LED, supports USB charging
- 5V (USB controller)
- 3.3V (IO, PERIPHERALS)
- 2.5V (VCCAUX, IO)
- 1.2V (CORE VOLTAGE)
- POWER-ON LED
- Power switch
- Standby voltage for RTC
- Reset supervision
- Jumper for selecting BANK4, BANK5 voltage

7) 34 independent I/O routed to the connectors, 7 high load IO outputs, i2c header
- One 2x12 male connector (22 IO, 1 GND, 1 VCC 3.3V or 2.5V)
- One 2x6 female connector (8 IO, 2 VCC 3.3V, 2 GND)
- One 1x6 female connector (4 IO, 1 VCC 3.3V, 1 GND)
- One 1x8 male connector (7 high load IO, 1 VCC)
- Max 50V AUX voltage and 500mA per output for high load IO
- Peripheral modules support
- 2.54mm pitch for all connectors
- One 1x4 male connector, i2c bus header (GND, VCC 3.3V, SCL, SDA)

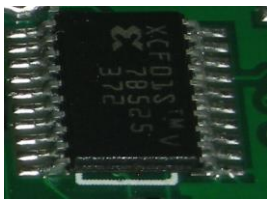
8) Small 100x100mm PCB

Instructions

1) XILINX XC3S200 is a FPGA, from SPARTAN-3 family. This FPGA, is good choice for most of beginners projects. It is big enough, to fit Microblaze embedded processor. This particular board has XC3S200 FT256 4C FPGA (256 ball package, speed grade 4, commercial temperature range 0°C to +85°C).

- SPARTAN-3 FPGA family datasheet: http://www.xilinx.com/support/documentation/data_sheets/ds099.pdf

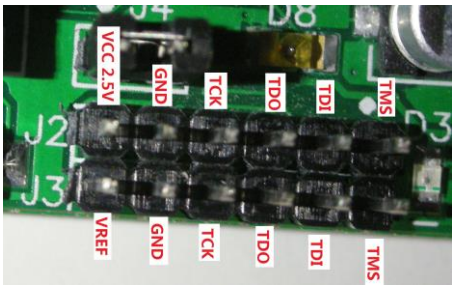
2) XILINX XCF01S VO20C is 1 Mbit platform Flash PROM with JTAG interface. There are 1,048,576 configuration bits in XCF01S Flash. XC3S200 FPGA requires 1,047,616. Demo design will be stored to flash during manufacturing. With this demo, most of the kit functions can be tested.



- Platform flash PROM user guide: http://www.xilinx.com/support/documentation/user_guides/ug161.pdf

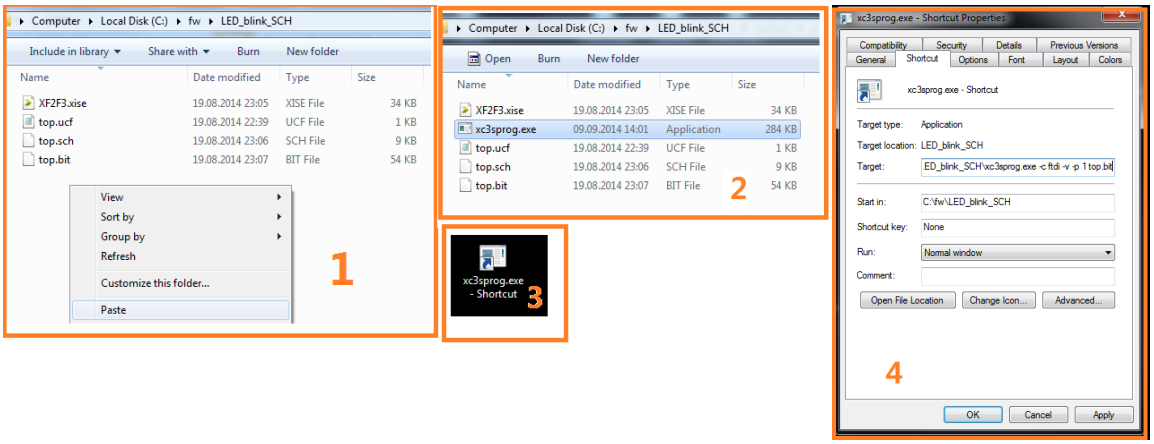
3) XKF3 FPGA kit has FTDI FT2232D USB controller onboard. PORT B of FT2232D is configured as UART interface. RX and TX signals are connected to FPGA pins D8 and C8. Demo design, what is stored in FLASH memory, demonstrates simple VHDL UART communication. Use these settings to establish UART connection: 9600-8-n-1. Demo project is designed so, that UART received data is transmitted back as echo. Received data is

monitored, XKF3 kit will respond with unique sound for symbols 0,1,2,3,4,5,6,7,8,9.
PORT A of FT2232D is configured as JTAG interface. It is connected to buffer IC's. They are needed to amplify driving current and to widen the supported voltage levels.
Buffer IC's are connected to J3 header. J2 header is connected to JTAG chain of FPGA and FLASH. By default, J2 is connected to J3, with jumpers, so that onboard programmer is connected to boards JTAG chain. If jumpers from J2 and J3 are removed, then, external JTAG devices can be connected to J3, for programming. Programmer can work with Vref from 1.65v to 5.5v. This includes 1.8v, 2.5v, 3.3v and 5v standard signal levels. You can program any JTAG device, not necessarily XILINX. Also, J2 connector can be used, when you want to program XKF3 kit with external programmer.

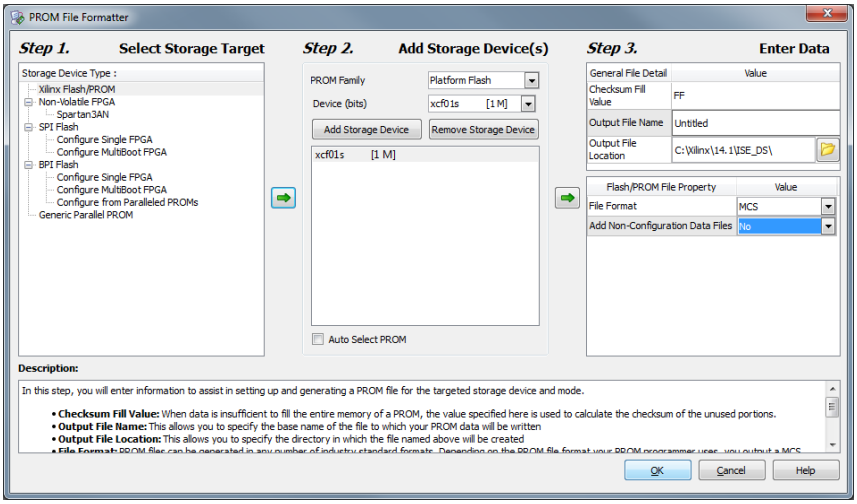


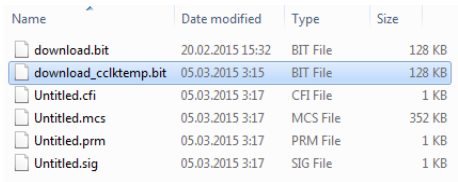
It is recommended to use program "XC3SPROG", for programming XKF3 kit.

1) Download xc3sprog.exe from https://svn.code.sf.net/p/xc3sprog/code/trunk/xc3sprog.exe
2) Place xc3sprog.exe to the folder of your ISE project, where .bit file is located.
3) Create shortcut on your desktop "C:\...\xc3sprog.exe -c ftdi -v -p 1 FILE_NAME.bit". Change "1" to "0", if you want to program FLASH instead of FPGA.
4) If something went wrong, or you want to explore more options, start "xc3sprog" from CMD.



In some cases, if your ".bit" file was created by XILINX PLATFORM STUDIO, instead of ISE, it may not work correctly, on hardware, if programmed with "xc3sprog". Follow these steps, to "fix" your ".bit" file, what is created in XPS, and not working on HW:
Start program "XILINX iMPACT" -> Press "launch wizard" -> "prepare a PROM file" -> "OK" -> "XILINX FLASH/PROM" -> platform flash xcf01s -> add storage device -> ok -> add your XPS .bit file -> close all pop up information windows -> operations -> generate file -> close iMPACT, no need to save changes to the project -> go to folder, what you specified as output file location -> find there file "… _cclktemp.bit" -> use it with xc3sprog, instead of your original ".bit" file.





Configuration for FT2232D is stored in 93c46 EEPROM. If something went terribly wrong, and onboard programmer is not working anymore, use FTDI's program "FT_Prog", to restore EEPROM configuration. You can find "FT.xml" file, in zip archive for this kit, it is XKF3 EEPROM content.

- FT2232D datasheet:
  http://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT2232D.pdf
- FTDI's program "FT prog":
  http://www.ftdichip.com/Support/Utilities/FT_Prog_v2.8.2.0.zip
- More info about FT2232D:
  http://www.ftdichip.com/Products/ICs/FT2232D.htm
- More info about XC3SPROG:
  http://xc3sprog.sourceforge.net/
- Alternative for XC3SPROG:
  http://urjtag.org/

4) Board has many peripherals onboard. This chapter contains information how to use, or test these peripherals, when factory demo design is loaded to FPGA.

- 4 yellow LEDs. LEDs D4, D5, D6 can be tested by rotating rotary encoder. D7 can be tested by switching the DIP switches.
- 4 active-low DIP switches with pull up resistors. When one of the switches is turned ON, speaker will produce beep sound and LED D7 will turn on.
- 16 ohm passive speaker. Can be tested by switching ON one of the DIP switches. Volume of the speaker can be adjusted, by changing supply voltage of BANK 5, with jumper J6. Caution: J6 jumper can be removed only when board main power switch is turned to OFF position. If using 2.5V, as IO voltage - don't forget to specify LVCMOS25, in the constrain file.
- CMOS 50MHz crystal oscillator. Your FPGA project may require other clock frequency. You can divide or multiply clock frequency by using XILINX Digital Clock Manager.
  More information about DCM:
  http://www.xilinx.com/support/documentation/application_notes/xapp462.pdf
- VGA port with resistor ladder DAC. Each color signal is separated to 3 IO pins with resistors. This scheme imitates the digital to analog converter. It can be used to gain more colors on the picture. With factory demo, VGA port produces 640x480 test signal with color bars.
- 16x2 Character LCD with HD44780, or functionally equal graphics controller. With factory demo, it is operated in 4-bit mode. Contrast of LCD can be adjusted with R37. With factory demo, backlight can be adjusted by rotary encoder.
  More information about LCD display:

http://www.allshore.com/pdf/Sunplus_LC780CV11.pdf
http://pldkit.com/download/HD44780.pdf

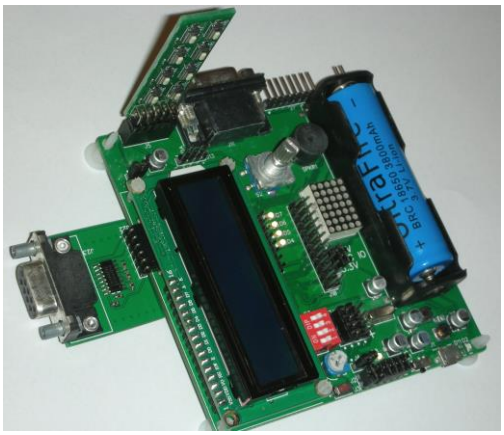
- Rotary Encoder with push button. Active-low, with pull up resistors. When rotated, LEDs are changing their state. When central push button is pressed, picoblaze soft processor core is in reset mode.
- 5x7 LED Matrix. With factory demo, it displays “HELLO” message.
  More information about LED Matrix:
  http://pldkit.com/download/BM-07K57ND.pdf
- Board has 4 optocoupled inputs, what are connected in parallel with DIP switches. These inputs can be used to connect high voltage signals or to avoid common ground. Also, can be used to avoid distortions, when mechanical sensor is connected by long wires. Maximum input voltage, for optocouler, is 6 volts. Voltage can be increased by adding additional resistors. You can select between “full isolation mode”, “common ground mode” and “common VCC mode” by changing jumpers on connectors J14, J15, J16 and J17.
- Board has 4 optocoupled outputs, what are connected in parallel with LEDs D4, D5, D6 and D7. They can be used to avoid common ground. For example, to drive keypad array on external device.
- AT24C256 256Kbit EEPROM. Message „XILINX FPGA KIT MODEL:XKF3 Rev.D“ is preprogrammed to EEPROM. This message is read and displayed on LCD, by picoblaze processor. EEPROM address on i2c bus is 1010111 (57).
  More information about AT24C256:
  http://www.atmel.com/Images/doc0670.pdf
- LM75 Temperature sensor. Picoblaze processor is reading temperature from sensor and display it on LCD. Red LED D10 is connected to LM75 overtemperature alarm output. By default, LED will turn ON, if sensor is heated till 80°C. This breakpoint can be adjusted. LM75 address on i2c bus is 1001000 (48).
  More information about LM75:
  http://datasheets.maximintegrated.com/en/ds/LM75.pdf
- PCF8563 Real time clock. Picoblaze processor is reading time from PCF8563 and display it on LCD. PCF8563 is powered from VCC MAIN. VCC MAIN remains active even if boards main switch is in the OFF position. Jumper J18 can be used to disconnect power from RTC. RTC address on i2c bus is 1010001 (51).
  More information about RTC:
  http://www.nxp.com/documents/data_sheet/PCF8563.pdf
- Board has 7 high load outputs, what are connected in parallel with LED matrix anodes. These outputs are made with ULN2003 Darlington transistor array, and can be used to connect stepper motor or relay, directly to the kit, without additional components. Jumper J8 is selecting voltage source for the output: VCC MAIN or VCC AUX. VCC AUX can be connected to J9. Maximum voltage for VCC AUX is 50 volts. When one of the high load outputs is enabled by FPGA - it is shorted to the GND by U12. So, you need to connect your load between U12 output (J7 pin2 – pin8) and VCC (J7 pin1). Maximum load is 500mA per output. Please pay attention, that “VCC AUX” voltage, what is mentioned here, is different from “FPGA VCCAUX 2.5V JTAG” voltage.
  More information about ULN2003:
  http://www.ti.com/lit/ds/symlink/uln2003a.pdf
- Board has 64Mbit HY57V64820HGT-H SDRAM. SDRAM memory is tested on factory, but PLDkit is not providing demo code for testing SDRAM features for users. You can try open source memory controllers, or maybe some of the paid solutions.
  More information about SDRAM memory:
  http://pldkit.com/download/HY57V64820HG.pdf

5) Red reset button BTN1 is connected to FPGA PROG_B signal. When it is pressed – RESET is active. As described in chapter 3, of this guide, XKF3 kit can be programmed by onboard USB programmer or by external JTAG programmer. D8 is FPGA DONE LED. It turns on after FPGA has finished configuration process. J4 is FPGA mode select jumper. When jumper is connected, all tree FPGA mode pins are tied to GND. This is Master Serial mode (loading from flash). When Jumper is removed, M0 and M2 pins are tied to VCC AUX by internal FPGA resistors, this is JTAG mode (waiting configuration from JTAG, not loading from the flash).

- More information about configuration modes, SPARTAN-3 datasheet, page 118: http://www.xilinx.com/support/documentation/data_sheets/ds099.pdf

6) XKF3 FPGA kit has standard micro-USB connector. You can use USB port or any micro-USB wall charger, to charge the battery. XKF3 FPGA kit has standard high capacity 18650 li-ion battery. XKF3 FPGA kit has LTC3455EUF power management IC, U3. Red LED D2 is charger status LED. When it lit – it means that charging is in process. Green LED D3 is power status LED. When it lit – it means that LTC3455 power outputs are enabled. S1 is main power switch. Filtered 5V, what is coming from USB connector, is used by USB controller and 93C46 EEPROM. 3.3V, what is produced by LTC3455, is used by FPGA IO, by onboard peripherals, and also supplied to IO connectors. 2.5V, what is produced by LTC3455, is used as FPGA VCCAUX JTAG voltage and also can be used ass VCCIO voltage for BANK4 and BANK5, if jumper J6 is in "2.5V" position. 1.2V is produced by LDO regulator from 3.3V, and used as FPGA core voltage. LTC3455 power controller also provides additional functions such as reset supervision and driver for LCD backlight. VCC MAIN voltage is used for powering RTC, and also can be used for the high load IO output.
More information about LTC3455:
http://cds.linear.com/docs/en/datasheet/3455fc.pdf

7) There are total 34 I/O pins, what are routed to the connectors, and can be used in your design. Please refer to the board schematics, to get information about connections. All I/O are independent and not crossing with any kit peripherals. J5 is 6x2 female connector. It has 8 IO, 2 VCC 3.3V and 2 GND. J19 is 6x1 female connector. It has 4 IO, 1 VCC 3.3V and 1 GND. These female connectors are designed specially to support peripheral modules. Peripheral modules,



with compatible male connectors, can be ordered from PLDkit web site, or from some other suppliers. J10 is 2x12 male connector. It has 22 IO, 1 GND, 1 VCC. VCC IO voltage for connector J10 can be selected between 3.3V and 2.5V, by using jumper J6. Caution: J6 jumper can be removed only when board main power switch is turned to OFF position. Please note that you must use I/O standard "LVCMOS33" or "LVTTL" if IO voltage is 3.3V, and "LVCMOS25" if IO voltage is 2.5V. Please note that HSWAP_EN pin is tied to VCCAUX, this means that when FPGA is not configured, all IO pull-up resistors are disabled. When demo design is loaded to FPGA, IO connectors can be tested. Use fly wire, to connect IO pins one by one to VCC. Test is passed if speaker beeps, every time when one of IO pins is connected to VCC. If there is missing contact or short circuit between IO, speaker will not beep. Be careful, and don't make short circuit between VCC and GND. J13 is i2c bus header, 1x4 male connector. It has GND, VCC 3.3V, SCL and SDA signals. It can be used to connect additional devices on i2c bus or to program EEPROM memory with external programmer. J7 is high load IO connector. It is 1x8 male connector, it has 7 high load IO and 1 VCC. Please read chapter 4, to get more information about

high load output. All connectors have 2.54mm pitch.

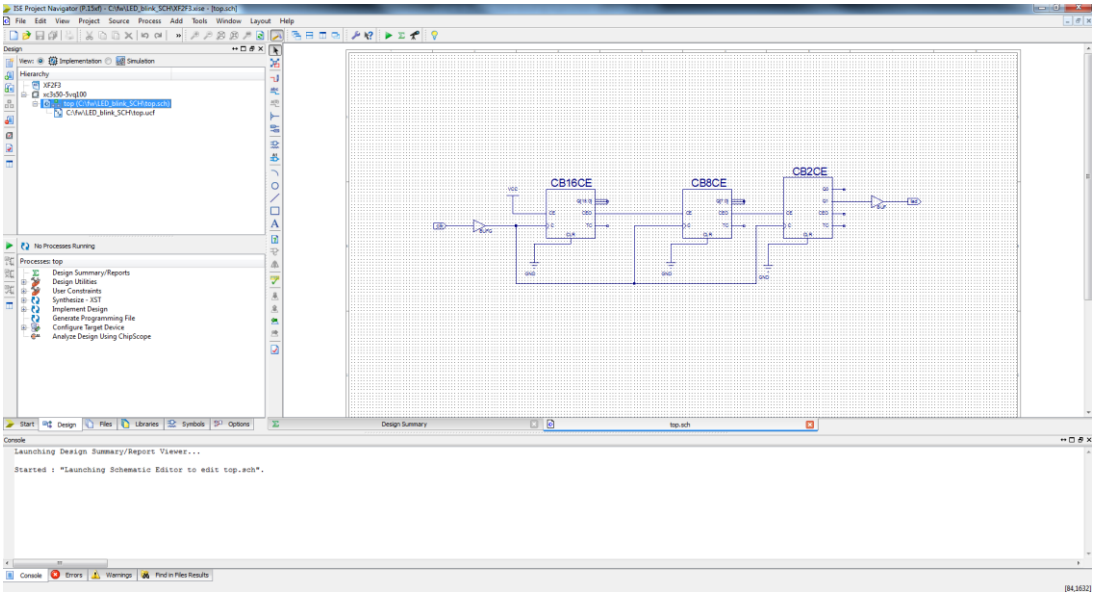
8) Board size is quite small – 100mm x 100mm. It can be easily carried from one location to another, or even mounted inside of some other device.

Quick start guide, for the first time user

1) Download and install Xilinx ISE (http://www.xilinx.com/support/download.html). Register, and get free license. Step by step instructions, in this guide, are referenced to ISE 14.1. If your version of ISE is different, some minor mismatches can be found. Also, demo projects for this kit, are created in ISE 14.1. It should be possible to open them in the newer ISE version.

2) Plug into USB port your XKF3 kit. Windows should find and install driver automatically, without any problems. If this did not happen, or you are not using windows, then, download drivers for FT2232D chip, from FTDI website (http://www.ftdichip.com/Products/ICs/FT2232D.htm). During driver installation, please note the COM port number, what was assigned to the kit. If you have missed that information, please find this information in computers device manager.

3) Zip archive, for this kit, has folder “fw”. In that folder, there are four folders with FPGA projects. Folder “demo” has demo design, what is stored to XKF3 flash. Project “iic_lcd” is for testing and debugging picoblaze system only. Two other projects are specially made for the first time user. These two projects are alike, but programmed differently. There are three ways, how to make a code, for XILINX FPGA. First way is to make schematics. You can just connect some logic components in the visual editor, and program this scheme to FPGA. Second way is to use VHDL language, to describe a logic scheme, instead of drawing it. And third way is to use Verilog language, to describe a logic scheme. Folder “LED_blink_SCH” has project with scheme, for blinking a led. Folder “LED_blink_VHDL” has project with VHDL code, for blinking a led. Let’s start with schematics. Go to “LED_blink_SCH” folder and open “XKF3.xise”. ISE project navigator will be opened. In the “Hierarchy” window, you can see files of the project. Below “Hierarchy” window, is “process” window. In “process” window, you can see what you can do with files from “Hierarchy” window. Double click on the file “top.sch” in “Hierarchy” window.



This will open file for editing. You can also edit file “top.ucf”. This file describes, to what pins, schematic will be connected. When you have finished editing, save changes, go to “process” window, right click on “Generate Programming File”, and select “run”. Two previous steps, “synthesize” and “implement design” will be run automatically. If there were no critical errors, then, you can find your generated programming file in “LED_blink_SCH” folder. In this example, it will have name “top.bit”. Please read chapter 3 of instructions guide, to get information about how to program your BIT file in to XKF3 kit. Follow same steps, when working with “LED_blink_VHDL” project. Instead of top.sch, open top.vhd, for editing VHDL code.