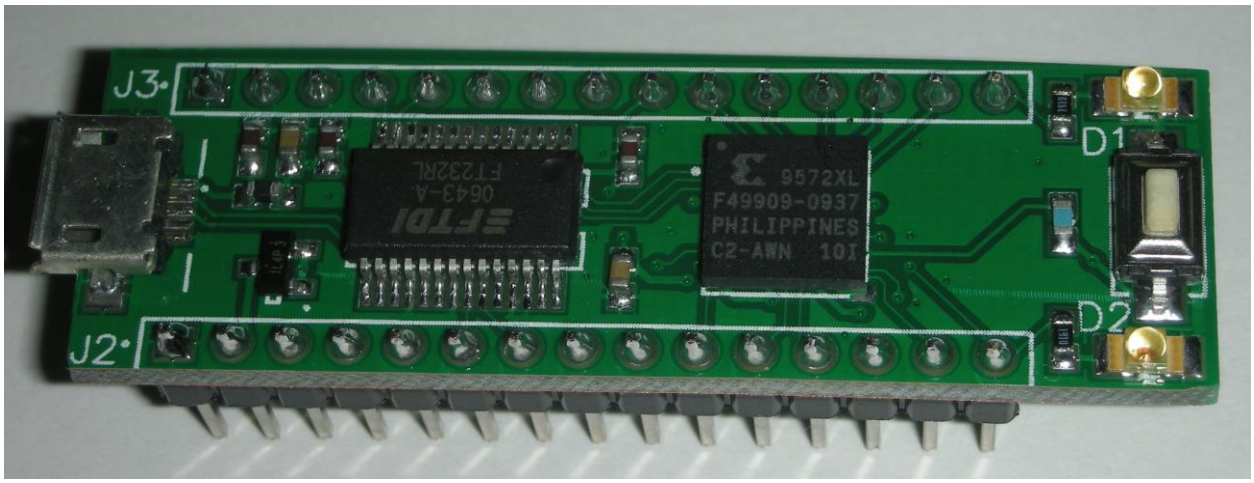
XILINX XC9500XL CPLD KIT USER's GUIDE

MODEL: XK2C95XL Revision A



Introduction

XK2C95XL CPLD kit is designed for developing small USB related projects. This kit doesn't require external power supply or programming adapter cable. Kit is powered from USB. Onboard USB controller allows JTAG programming, provides clock for CPLD, and also has other options. Kit has few basic onboard peripherals for simple projects.

Features

1) XILINX XC9572XL CS48 10I CPLD
- 1600 gates (72 macrocells)
- 38 User I/O (26 routed on this board)
- System frequency up to 178 MHz
- 5 ns pin-to-pin logic delays
- Low power operation
- 5V tolerant I/O pins accept 5V, 3.3V and 2.5V signals
- 3.3V or 2.5V output capability (3.3V on this board)
- Enhanced data security features
- IEEE Standard 1149.1 Boundary-Scan (JTAG)
- Endurance of 10000 Program/Erase Cycles
- 20 year data retention
- ESD protection exceeding 2000V
- Fully supported by latest XILINX design tools

2) FTDI FT232RL USB controller
- Bit-banged USB JTAG programming
- 3.3V regulator
- Entire USB protocol handled on the chip
- Integrated EEPROM
- Integrated clock generation
- Configurable CBUS I/O pins
- Configurable I/O pin output drive strength

3) Onboard IO peripherals
- 2 LEDs
- 1 push button

4) Onboard power supply
- Kit is powered from USB
- 5V
- 3.3V

5) I/O routed to the connectors
- Two 15-pin male connectors (13 IO, 1 VCC, 1 GND)
- 2.54mm pitch for all connectors
- 5V tolerant CPLD I/O pins accept 5V, 3.3V and 2.5V signals

6) Small and handy PCB layout

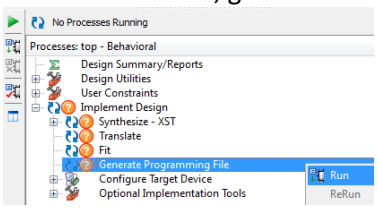
Instructions

1) XILINX XC9572XL is a CPLD, from XC9500XL family. This particular board has XC9572XL CS48 10I CPLD (48 ball package, speed grade 10, industrial temperature range -40°C to +85°C).

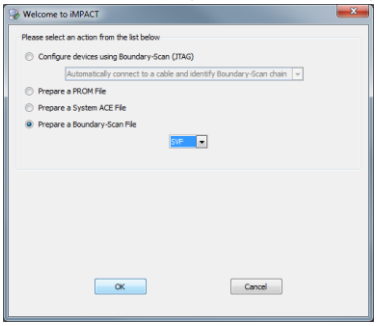
- XC9500XL CPLD family datasheet:
  http://www.xilinx.com/support/documentation/data_sheets/ds054.pdf

2) XK2C95XL CPLD kit has FTDI FT232RL USB controller onboard. FT232RL has internal 3.3V voltage regulator. 3.3V voltage is used by FT232RL, by CPLD, and supplied to I/O connectors. Maximum current, what can provide FT232RL on 3.3V, is 50mA. FT232RL has internal oscillator and clock multiplier. It can be programmed to output these clock signals on CBUS. By default, CBUS of XK2C95XL kit is programmed in this way:
CBUS0 – CLK6MHz,
CBUS1 – CLK12MHz,
CBUS2 – CLK24MHz,
CBUS3 – CLK48MHz,
CBUS4 – CLK6MHz.
CBUS4 is connected to CPLD GCK2, pin B6, it is used as main clock. Other CBUS signals are also connected straight to CPLD. FT232RL has internal EEPROM memory for storing configuration. ZIP archive, for this kit, contains file "XK2C95XL.xml", this is default EEPROM configuration of XK2C95XL CPLD kit. It can be programmed and customized with FTDI's program "FT_Prog". There are many customizable options, including CBUS configuration.
FTDI chip is connected to CPLD's JTAG port for bit-bang programming.
Here are step by step instructions, how to program XK2C95XL CPLD kit:

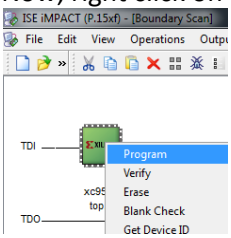
- In XILINX ISE suite, generate .JED programming file, for your project.



- Run ISE iMPACT, launch wizard, select "Prepare a Boundary-Scan File", "SVF". Press "OK".



- Type file name, select location, and press "Save"
- In next window, locate .JED file, what you made in ISE design suite.
- Now, right click on CPLD picture, and select "program"



- Window with device programming properties should appear now. Unselect “verify”, select “design-specific erase before programming”. Press “OK”

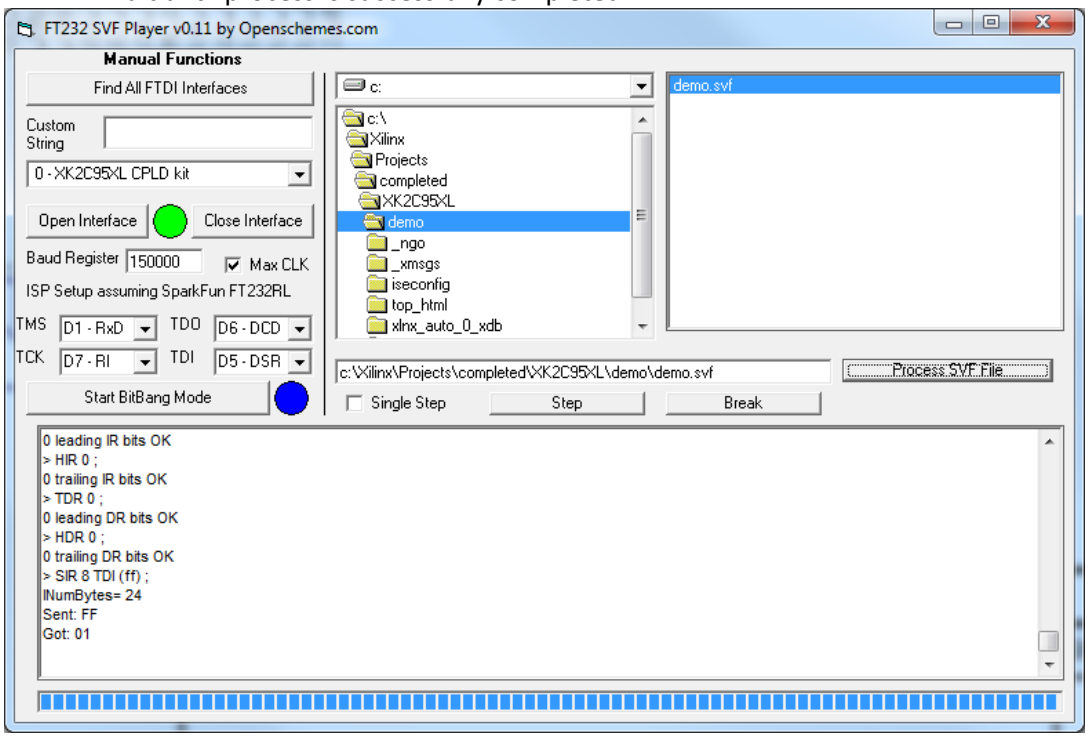
Property Name	Value
Verify	☐
General CPLD And PROM Properties	
Design-Specific Erase Before Programming	☑
Read Protect	☐
CPLD Specific Properties	
Write Protect	☐
Functional Test	☐

- When “Program Succeeded” is displayed, close iMPACT. No need to save the project.

- Now we have .SVF file, what includes all activity, what was made in iMPACT. We need to “play” this file in FTDI bit-bang mode. It is recommended to use program “Openschemes FT232 JTAG SVF Player”, for that.
- Download FT232 SVF Player from here:

http://openschemes.com/wp-content/uploads/2011/10/Openschemes_FT232_SVF_Player_v0.11.zip

- Plug XK2C95XL kit to USB. Unzip the archive and run “FT232SVF.exe”
- Delete everything from the “Custom String” field. Press “Find all FTDI Interfaces”. Locate “XK2C95XL CPLD kit”, and press “Open Interface”. Press “Start BitBang Mode”. Navigate to the folder, where .SVF file is located. Select .SVF file. Uncheck “single step”. Press “Process SVF file”. Wait until process is successfully completed.



If process fails, try to connect XK2C95XL CPLD kit straight to USB port, without USB extenders and USB hubs. If it fails again, try lower Baud Rate.

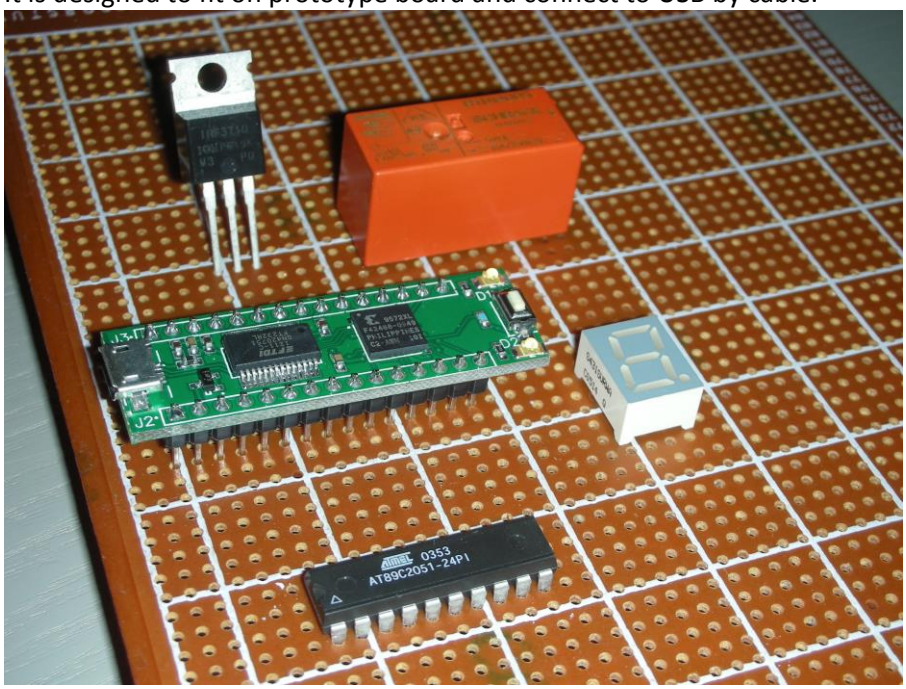
- FT232RL datasheet: http://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT232R.pdf
- FTDI's "FT prog" utility: http://www.ftdichip.com/Support/Utilities/FT_Prog_v2.8.2.0.zip
- More info about FT232RL: http://www.ftdichip.com/Products/ICs/FT232R.htm
- More info about “Openschemes FT232 JTAG SVF Player”: http://openschemes.com/2011/10/28/ft232-bit-bang-jtag-programmer-revision-0-11

3) Board has few simple peripherals onboard: 2 yellow LEDs (C7, E7), 1 momentary active-low push button with pull up resistor (G6). As described in previous chapter, board uses clock signal from USB controller. Be aware, that if USB suspend mode is activated or if you are not using USB port, to power XK2C95XL CPLD kit, all clock signals, from USB controller, will be disabled. If your project requires clock signal, when board is not powered by USB, you should connect external oscillator to CPLD GCK1 or GCK3 pins (J3-14 or J3-13).

4) XK2C95XL kit is designed to receive power from USB port, but in some cases, it can be powered by other, 5V power source, connected to J3-2. Filtered 5V is used by USB controller. As described in previous chapter, FT232RL provides 3.3V, but maximum current is only 50mA. If more current is required, use external voltage regulator, or use 5V. Input pins of CPLD are 5V tolerant, even if CPLD is powered by 3.3V.

5) There are total 26 CPLD I/O pins, and 5 FTDI I/O pins, what are routed to the connectors, and can be used in your design. Please refer to the board schematics, to get information about connections. Some I/O pins are crossing with kit peripherals. J2 and J3 are 15x1 male connectors. Each connector has 13 I/O, 1 GND and 1 VCC, 5V or 3.3V. All connectors have 2.54mm pitch. Board can be fitted to standard 2.54mm prototype board. 5V tolerant CPLD I/O pins accept 5V, 3.3V and 2.5V signals. Since CPLD VCCIO is powered by 3.3V, output voltage level from CPLD I/O is 3.3V. Output voltage level from FTDI I/O pins is 5V, maximum current is set to 12mA per pin. Maximum current can be changed to 4mA in “FT prog” utility.

6) Board size is small and handy.
It is designed to fit on prototype board and connect to USB by cable.



Powering up the board for the first time

1) Connect XK2C95XL CPLD kit in to USB port.
2) Wait until driver is installed automatically. If this did not happened, download FT232 driver here: http://www.ftdichip.com/Products/ICs/FT232R.htm
3) Demo design will be automatically loaded, when USB connection is established.
4) IO LEDs will start blinking. This process can be stopped with button BTN1.