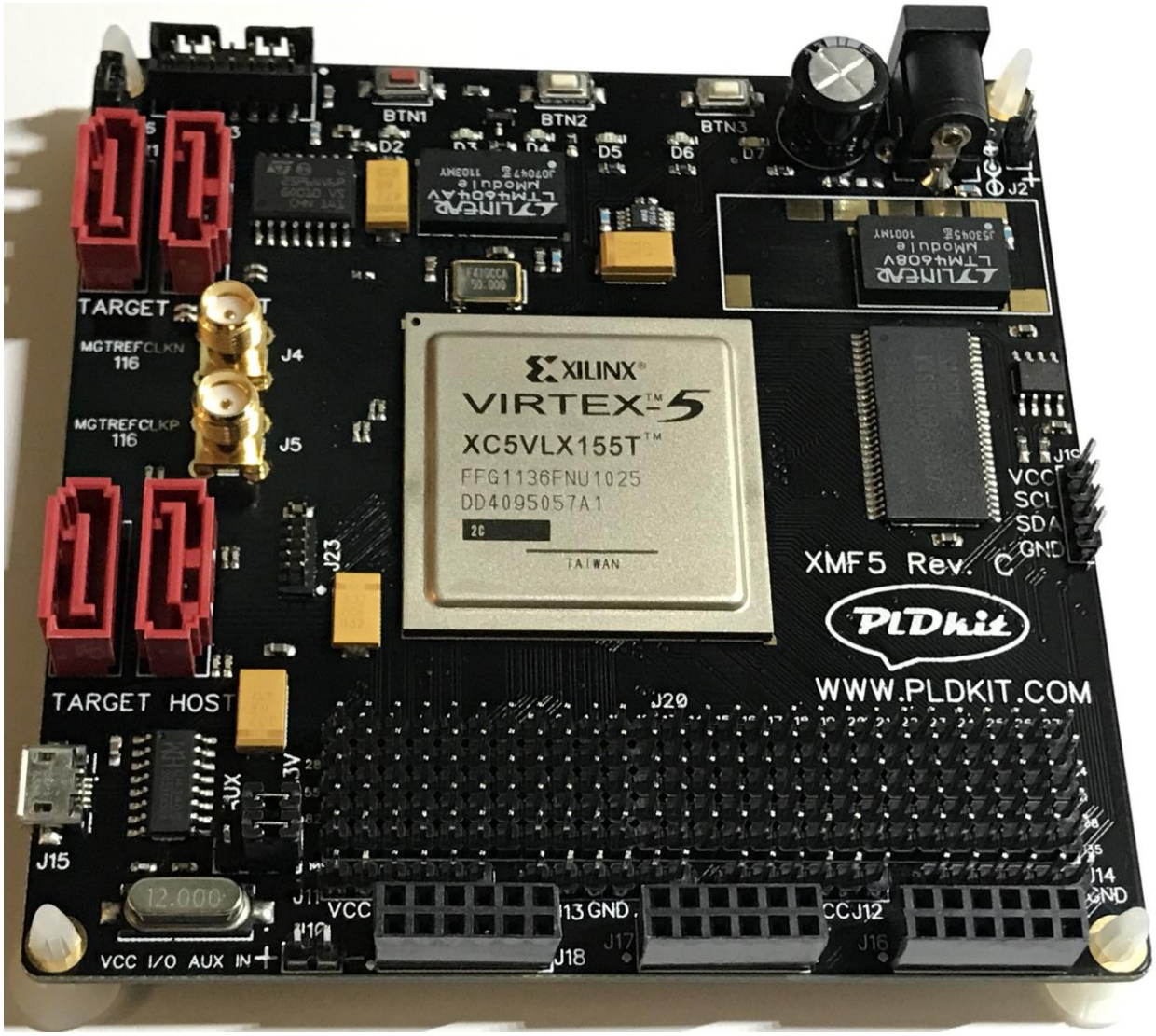
XILINX VIRTEX-5 FPGA MODULE USER's GUIDE

MODEL: XMF5-155-64-256 50/75M Revision C



Introduction

Xilinx Virtex-5 XMF5 FPGA module is designed for rapid prototyping and implementing FPGA projects. Module can be used for educational purposes. Module can work independently, or as control module in the bigger design.

Features

1) XILINX XC5VLX155T FFG1136 2C FPGA
- 24320 Virtex-5 Slices (155648 Logic Cells)
- 128 DSP48E Slices
- 212x 36Kb RAM blocks (7632Kb, 550MHz)
- 6 Clock Management Tiles
- 1 Endpoint Block for PCI Express
- 4 Ethernet MACs
- 16 GTP RocketIO 3.75 Gb/s Transceivers (6 routed on this board)
- 640 User I/O (211 routed on this board)

2) ST M25P64 SPI Flash
- 64Mbit
- SPI Bus Interface
- FPGA configuration
- Post-configuration access
- More than 100000 Program/Erase Cycles and 20-year data retention

3) Onboard IO peripherals
- 256Mbit 133MHz SDRAM
- 256Kbit EEPROM
- CH340G USB UART port
- 50MHz CMOS oscillator for IO
- 75MHz LVPECL oscillator for Rocket IO
- Four IO LEDs
- Two IO push buttons

4) RocketIO Transceivers
- 2x SATA HOST port
- 2x SATA TARGET port
- One MGT clock input routed to SMA connectors
- Two transceivers routed to 1.27mm male header

5) Handy configuration
- 14-pin JTAG header
- Indirect Programming of SPI Flash
- Mode select jumper (JTAG or FLASH)
- Push button for manual initiation of configuration process
- Reset supervision by voltage monitor
- DONE LED

6) Onboard power supply
- 3.3V 4A (IO, PERIPHERALS)
- 2.5V 1.5A (VCCAUX)
- 1V 8A (CORE VOLTAGE)
- 1.2V 1.5A (Rocket IO)

- Input voltage range 4.5V – 5.5V
- POWER-GOOD LED
- AUX input for I/O voltage 1.14V-3.45V

7) 161 I/O routed to the connectors
- 15 differential pairs with matched PCB tracks
- 6x27 male pin array, 135 I/O with selectable voltage level
- Three 2x6 female connectors, 24 I/O with selectable voltage level
- Peripheral modules support
- 2.54mm pitch for all connectors
- I²C header
- Test points for FPGA temperature diode

8) Small 100x100mm PCB with M3 mounting holes

Instructions

1) The Virtex-5 family provides the newest most powerful features in the FPGA market. In addition to the most advanced, high-performance logic fabric, Virtex-5 FPGAs contain many hard-IP system level blocks. These features allow advanced logic designers to build the highest levels of performance and functionality into their FPGA-based systems. Built on a 65-nm state-of-the-art copper process technology, Virtex-5 FPGAs are a programmable alternative to custom ASIC technology. This particular board has XC5VLX155T FFG1136 2C FPGA (1136 ball package, speed grade 2, commercial temperature range 0°C to +85°C.

- Virtex-5 Family Overview:
  http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
- Virtex-5 FPGA DC and Switching Characteristics:
  http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf
- Virtex-5 FPGA User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
- Virtex-5 FPGA Configuration User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug191.pdf
- Virtex-5 FPGA XtremeDSP Design Considerations:
  http://www.xilinx.com/support/documentation/user_guides/ug193.pdf

2) U8 is M25P64 64Mb ST SPI flash IC. 64Mb is more than required for XC5VLX155T single bitstream. After FPGA is configured, free space can be used by embedded processor. Demo design will be stored to flash, to test all of the module peripherals. Because SPI is a serial interface, and bitstream for XC5VLX155T is quite big, it is taking 14 seconds to load bitstream, after board is powered on.

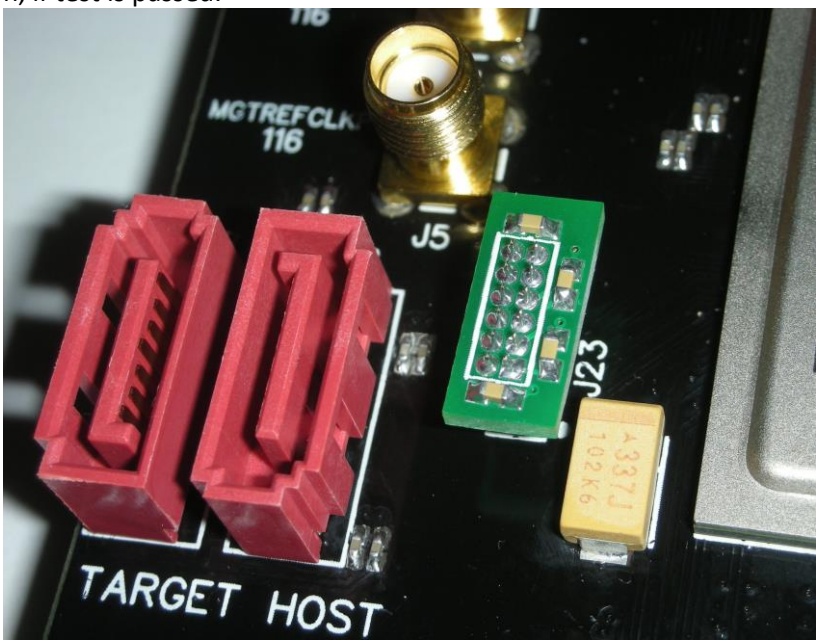
- M25P64 datasheet:
  http://pldkit.com/download/M25P64.pdf
- Post-Configuration Access to SPI Flash Memory with Virtex-5 FPGAs:
  http://www.xilinx.com/support/documentation/application_notes/xapp1020.pdf

3) Board has few simple peripherals onboard. 4 yellow LEDs, pins B12, A13, B13 and C13. Two active-low push buttons, pins G13 and E13. Board has CH340G USB UART port. J15 is micro-USB connector, located at the bottom left corner of the board. RX and TX are connected to AG12 and AF16. Use these settings to establish UART connection: 115200-8-n-1. Board is equipped with 50 MHz CMOS crystal oscillator, connected to pin G15, and 75MHz LVPECL oscillator, connected to MGT_112 tile. You can use DCM to divide or multiply clock

frequency. Additional clock signals can be connected from outside.
XMF5 module has 256Mbit 133MHz K4S561632J-UC75 SDRAM memory, and AT24C256 256Kbit EEPROM. All these peripherals can be tested when VHDL demo project is loaded to FPGA. VHDL demo project includes “reprogramming mode”. In this mode, EEPROM can be reprogrammed. To program AT24C256, connect external programmer to J19. To restore EEPROM factory settings, use “xmf5_c.bin”. J19 connector also can be used to connect logic analyzer, to debug your projects.

- CH340G datasheet and driver:
  http://pldkit.com/download/CH340.zip
- K4S561632J-UC75 datasheet:
  http://pldkit.com/download/K4S561632J.pdf
- AT24C256 datasheet:
  http://www.atmel.com/Images/doc0670.pdf
- LogiCORE IP Multi-Port Memory Controller:
  http://www.xilinx.com/support/documentation/ip_documentation/mpmc/v6_05_a/mpmc.pdf

4) Board has 3 GTP_DUAL tiles routed, what gives 6 GTP RocketIO Transceivers. There is 75MHz LVPECL oscillator and two SATA ports, connected to MGT_112 tile. Any of onboard transceivers can be clocked from this 75MHz oscillator. Transceivers also can be clocked from FPGA I/O clock. J22 and J8 are SATA HOST ports. Peripherals like SATA hard drive, can be connected there. J21 and J7 are SATA TARGET ports. External SATA controller can be connected there, and XMF5 will act as SATA peripheral. You can still use TARGET port as HOST, or HOST port as TARGET, if connect SATA crossover cable, instead of ordinary. There are two SMA connectors and two SATA ports, connected to MGT_116 tile. External differential clock signal can be connected to J4 and J5. Both transceivers of MGT_114, including MGTREFCLK pins, are routed to J23, 1.27mm pitch male connector. J23 also has GND and VCC 3.3V pins. Additional modules, like Ethernet PHY can be connected, and powered, from J23. When demo design is loaded to FPGA, transceivers can be tested, by looping one to another. To test MGT_112, connect J22 to J21 with SATA cable. LED D5 will turn on, if test is passed. To test MGT_116, connect J8 to J7 with SATA cable. LED D6 will turn on, if test is passed. To test MGT_114, connect 12-pin loop test accessory, to J23. LED D4 will turn on, if test is passed.



Demo design includes Chipscope core. To use it, load design, and connect to FPGA with Chipscope Pro Analyzer 14.1.

- Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide: http://www.xilinx.com/support/documentation/user_guides/ug194.pdf
- Virtex-5 FPGA RocketIO GTP Transceiver User Guide: http://www.xilinx.com/support/documentation/user_guides/ug196.pdf
- LogiCORE IP Virtex-5 FPGA RocketIO GTP Transceiver Wizard v2.1: http://www.xilinx.com/support/documentation/ip_documentation/v5_gtpwizard_ds590.pdf
- LogiCORE™ IP Virtex®-5 FPGA RocketIO™ GTP Transceiver Wizard v2.1 Getting Started Guide: http://www.xilinx.com/support/documentation/ip_documentation/v5_gtpwizard_gsg188.pdf
- Serial ATA Physical Link Initialization with the GTP Transceiver of Virtex-5 LXT FPGAs: http://www.xilinx.com/support/documentation/application_notes/xapp870.pdf

5) J3 is JTAG connector, it has 14 pins, with pitch 2mm. This is standardized XILINX JTAG connector. Only FPGA IC is connected straight to J3. To program SPI flash, indirect SPI flash programming method should be used. iMPACT version 14.1 should be used, to program M25P64 on XMF5. Newer versions of iMPACT are not tested, and not guaranteed to work reliably with this board. J6 is FPGA mode select jumper. When jumper is connected, master SPI mode is selected (M[2:0] = <0:0:1>). In this mode, FPGA is loading configuration from SPI flash. When Jumper is removed, JTAG mode is selected (M[2:0] = <1:0:1>). Make sure, that during flash indirect programming jumper is installed. Otherwise, you may get error “DONE pin did not go high”. Red button BTN1 is connected to FPGA PROGRAM_B signal. When it is pressed – FPGA is forced to start reconfiguration process. To configure or reconfigure FPGA from FLASH, insert J6 jumper and press BTN1 button. To clear FPGA configuration and put it in JTAG mode – remove J6 jumper and press BTN1 button. PROGRAM_B also can be pulled low by U4, MAX809TEUR voltage monitor. The function of the MAX809 is to monitor the 3.3v VCC supply voltage, and assert a PROGRAM_B signal low whenever this voltage declines below the 3.08v reset threshold. The reset signal remains asserted for 240ms after VCC rises above the threshold. This ensures that during power on, flash will be ready before FPGA, for proper bitstream loading.
D2 is FPGA DONE LED. It turns on, after FPGA has finished configuration process.

- Configuring Xilinx FPGAs with SPI Serial Flash: http://www.xilinx.com/support/documentation/application_notes/xapp951.pdf
- MAX809 datasheet: http://datasheets.maximintegrated.com/en/ds/MAX803-MAX810Z.pdf

6) Board has powerful power supply, to serve the needs of VIRTEX-5 FPGA. Core voltage for FPGA is provided by LTM4608V. Together with 1980uF tantalum capacitors, it is very stable, accurate, and powerful solution. LTM4608V can deliver up to 8A current for FPGA core. Peak current can be up to 10A. 3.3V supply is built with LTM4604AV, highly integrated and efficient DC-DC converter. Maximum continuous output current from LTM4604AV is 4A. Peak current can be up to 5A. Output 3.3V is used by board peripherals, and by FPGA IO banks. 2.5V supply and 1.2V supply are built with two MIC49150, high-bandwidth, low-dropout, LDO regulators. Maximum output current from MIC49150 is 1.5A. 2.5V is used for FPGA VCCAUX. 1.2V supply is used for FPGA GTP transceivers. Board has J10 connector - AUX I/O voltage input. Input voltage range is 1.14V-3.45V. If voltage, what is above the maximum limit is applied to J10, FPGA IC will be permanently damaged. Supply voltage for banks 18,22,4,21,17,13,19,15 can be selected between 3.3V and J10 VCC AUX, with J9 jumpers. If some of these banks will have huge load, it is recommended to replace jumpers with solder bridges, to achieve better current flow.
J1 jack is used to connect DC power adapter. Also, two-pin header J2 can be used, for low load designs. Be careful with voltage polarity. There is protective diode D1, to protect from wrong polarity and overvoltage, but it has limited abilities. External power supply voltage must be within range of 4.5V to 5.5V, and capable to provide at least 1.5A current, to test all functions of the demo design. Much bigger current may be required, for your custom FPGA design.

D7 is a POWER-GOOD LED. When it is on, it means that 3.3V output from LTM4604 is within ±7.5% of the regulation point and 1V output from LTM4608 is within ±10% of the regulation point.

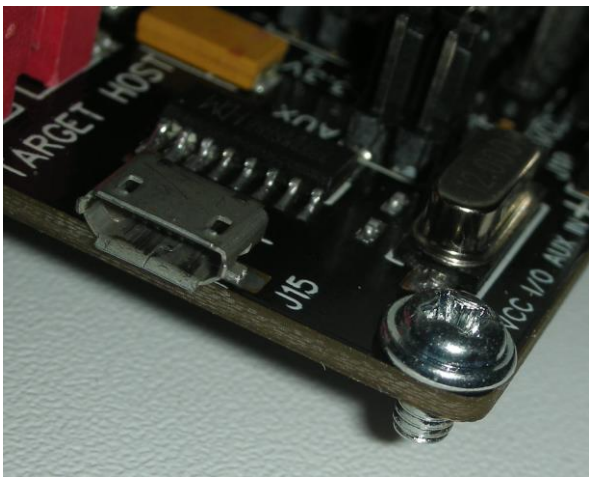
7) There are total 159 I/O pins, what are routed to the connectors, and can be used in your design. Please refer to the board schematics, to get information about connections. All these I/O are independent and not crossing with any module peripherals. J20 is 135 male pin array. It is divided to four groups: 1 to 7 column - BANK18 + BANK22, 8 to 11 column - BANK4, 12 to 19 column - BANK17 + BANK21, 20 to 27 column - BANK13.
J16, J17 and J18 are 6x2 female connectors. J18 and J17 routed to BANK19, J16 to BANK15. Each connector has 8 IO, 2 VCC and 2 GND. These female connectors are designed specially to support peripheral modules. Peripheral modules, with compatible male connectors, can be ordered from PLDkit web site, or from some other suppliers.
Supply voltage for banks can be set separately with J9 jumpers, 3.3V or 1.14V-3.45V from J10 VCC AUX. Caution: J9 jumpers can be removed only when board is turned OFF.
J11 is VCC IO power connector, corresponding to banks 4, 15, 18, 19, 22. J12 is VCC IO power connector, corresponding to banks 13, 17, 21. J13 and J14 are GND connectors.
Please note that you must use I/O standard “LVCMOS33” or “LVTTL”, when IO voltage is set to 3.3V. Please note that HSWAPEN FPGA pin is connected to GND, this means that when FPGA is not configured, all IO pull-up resistors are enabled.
When demo design is loaded to FPGA, IO connectors can be tested. Use fly wire, to connect IO pins one by one to BANK VCC. Test is passed if LEDs were turning on, every time when one of IO pins is connected to VCC. If there is missing contact, or short circuit between IO, then LEDs will not turn on. Be careful, and don’t make short circuit between VCC and GND. Also don’t connect main 5V voltage to IO pins.
This board has 15 differential IO pairs routed. Positive and negative track of each pair are routed side-by-side, and their length is matched.
Here is a list of differential pairs, what are properly routed on this board:

IO_L0P_GC_D15_4 + IO_L0N_GC_D14_4 = AG22 + AH22 = J20 PIN119 + J20 PIN92 (BANK4)
IO_L1P_GC_D13_4 + IO_L1N_GC_D12_4 = AH12 + AG13 = J20 PIN35 + J20 PIN8 (BANK4)
IO_L8P_CC_GC_4 + IO_L8N_CC_GC_4 = AF18 + AE18 = J20 PIN10 + J20 PIN37 (BANK4)
IO_L19P_13 + IO_L19N_13 = AN32 + AP32 = J20 PIN74 + J20 PIN47 (BANK13)
IO_L15P_13 + IO_L15N_13 = AJ32 + AK32 = J20 PIN128 + J20 PIN101 (BANK13)
IO_L11P_CC_13 + IO_L11N_CC_13 = AD32 + AE32 = J20 PIN103 + J20 PIN130 (BANK13)
IO_L2P_18 + IO_L2N_18 = AA5 + AB5 = J20 PIN28 + J20 PIN1 (BANK18)
IO_L10P_CC_18 + IO_L10N_CC_18 = AG5 + AF5 = J20 PIN110 + J20 PIN83 (BANK18)
IO_L18P_18 + IO_L18N_18 = AK7 + AK6 = J20 PIN59 + J20 PIN32 (BANK18)
IO_L19P_21 + IO_L19N_21 = AD24 + AE24 = J20 PIN97 + J20 PIN124 (BANK21)
IO_L13P_21 + IO_L13N_21 = AF24 + AG25 = J20 PIN70 + J20 PIN43 (BANK21)
IO_L0P_22 + IO_L0N_22 = AN14 + AP14 = J20 PIN88 + J20 PIN115 (BANK22)
IO_L8P_CC_22 + IO_L8N_CC_22 = AL11 + AL10 = J20 PIN60 + J20 PIN33 (BANK22)
IO_L13P_22 + IO_L13N_22 = AK8 + AK9 = J20 PIN86 + J20 PIN113 (BANK22)
IO_L12P_VRN_22 + IO_L12N_VRP_22 = AF8 + AE9 = J20 PIN30 + J20 PIN57 (BANK22)

There are more differential pairs on this board, but PCB tracks are not matched for them.
J19 is I²C header, connected in parallel to boards I²C bus. J19 can be used to reprogram EEPROM, or to connect logic analyzer. All connectors have 2.54mm pitch.
Internal FPGA thermal diode is routed to test points TP2 (DXP_0) and TP1 (DXN_0).
By connecting this diode to an external signal conditioning IC (thermal monitor), the die temperature could be determined. With some designs, FPGA can heat quite fast. Adhesive heatsink can be mounted on top of FPGA. FPGA system monitor is disabled on this board.

- Peripheral modules:
  http://pldkit.com/peripheral-modules
- Virtex-5 FPGA System Monitor User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug192.pdf

8) Board size is quite small – 100mm x 100mm. It can be mounted inside of some other device. Every corner of the PCB has metalized 3.1MM mounting hole, connected to GND. You can use M3 bolts and spacers, to fasten XMF5 on some surface.



Powering up the board for the first time

1) Connect 5V 2A to J1, with correct polarity.

2) Demo design will be automatically loaded into FPGA from the Flash, if jumper J6 is not removed. Loading will take 14 seconds.

3) LEDs D3-D6 will start blinking. Red power LED and green DONE LED must be constantly ON.

4) Connect XMF5 to your computer with micro-USB cable. Install drivers. Establish UART terminal connection with settings 115200-8-n-1.

5) Press BTN2 to reset system, or BTN1 to reload bitstream.

6) You will see welcome message in the UART terminal.

7) Press “1” to execute RAM test. Results will be sent to UART. System will switch back to main menu, when RAM test is over. LEDs D3-D6 will indicate process progress (25%,50%,75%,100%).

8) Press “2” to enter EEPROM reprogramming mode. In this mode EEPROM is not used by the system, and can be reprogrammed by external programmer. LEDs D3 and D4 indicate status of SCL line. LEDs D5 and D6 indicate status of SDA line. Connect external programmer to J19. Use xmf5_c.bin to restore EEPROM factory settings. Press BTN2 or BTN1 when finished, to switch back to main menu.

9) Press “3” to enter IO test mode. In this mode J16,J17,J18,J20 and BTN3 can be tested. Connect IO pins to VCC_3.3V one by one, or press BTN3. If one IO pin is connected to VCC - all LEDs will turn ON. If none, or several pins are connected at the same time - LEDs will stay OFF. System will switch back to main menu after 10 minutes, or if BTN2 or BTN1 is pressed.

10) Press “4” to enter GTP transceivers test mode. Current consumption and heat dissipation of the board will increase twice, when you will enter this mode. In this mode J7,J8,J21,J22,J23 and LVPECL oscillator can be tested. Connect J7 to J8 with SATA cable. Connect J21 to J22 with SATA cable. Connect J23 loop test accessory to J23 connector. If D3 is ON, LVPECL oscillator test is PASSED. If D4 is ON, J23 (MGT 114) test is PASSED. If D5 is ON, J21&J22 (MGT 112) test is PASSED. If D6 is ON, J7&J8 (MGT 116) test is PASSED. Use ChipScope Analyzer to observe transceiver signals. System will switch back to main menu after 10 minutes, or if BTN2 or BTN1 is pressed.

11) Press “5” to execute SPI flash test. Test results will be sent to UART. Test will be PASSED, if SPI ID is 20h 20h 17h.

Model name chart