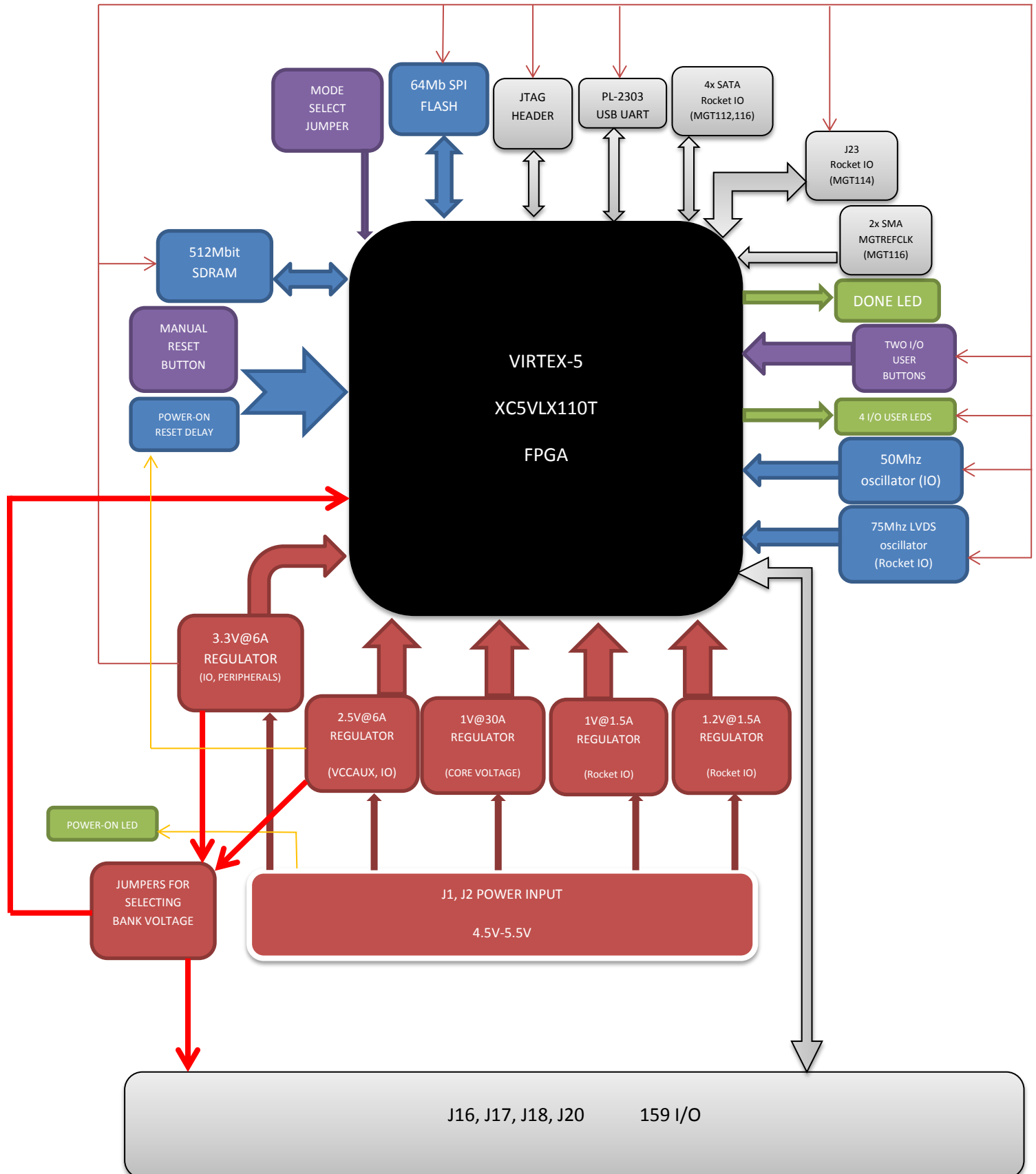
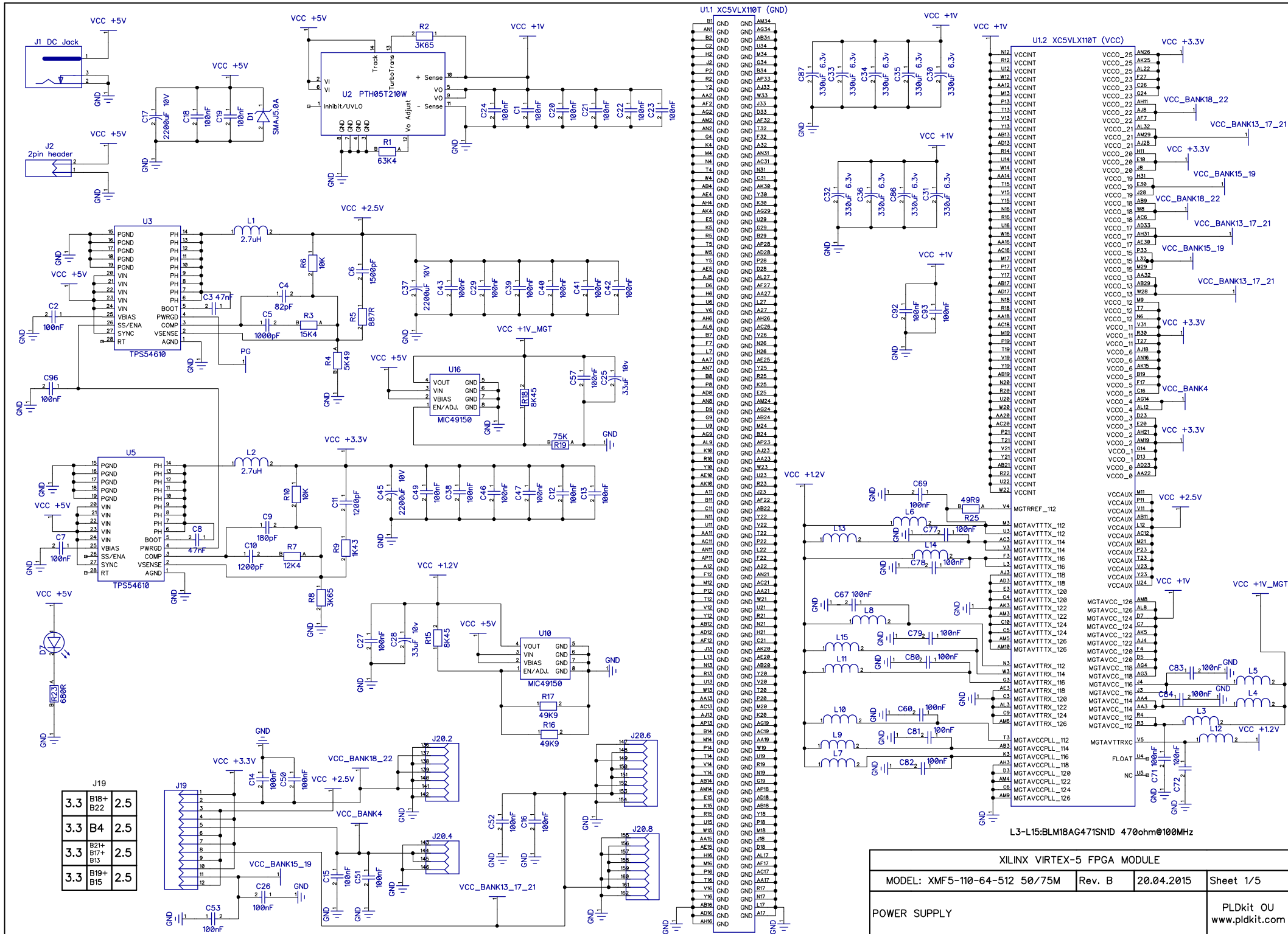
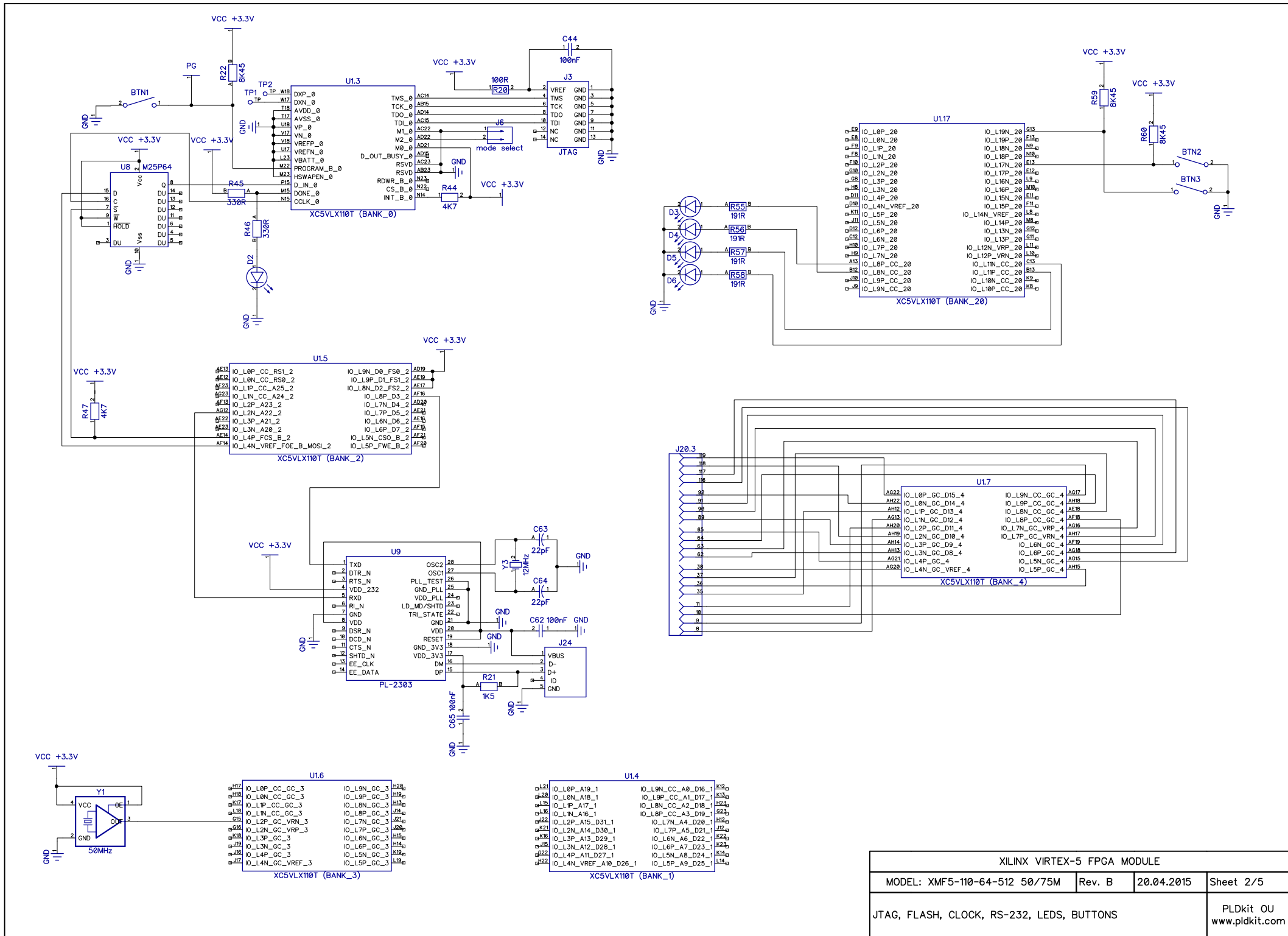


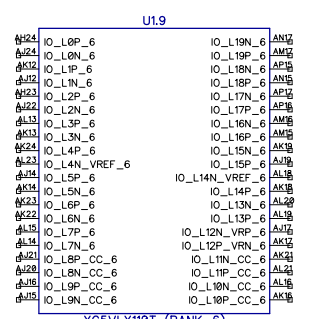
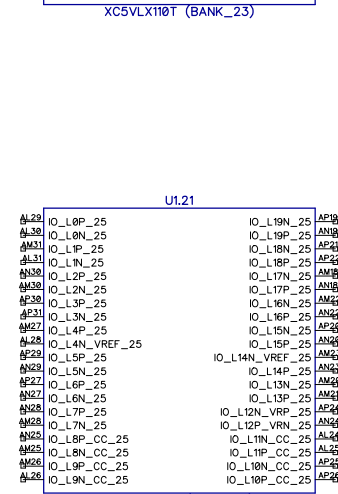
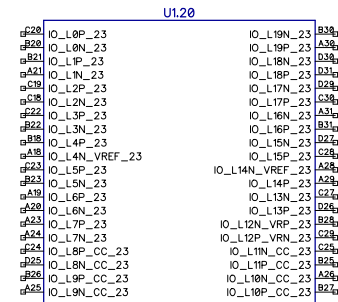
# XILINX VIRTEX-5 FPGA MODULE BLOCK SCHEME

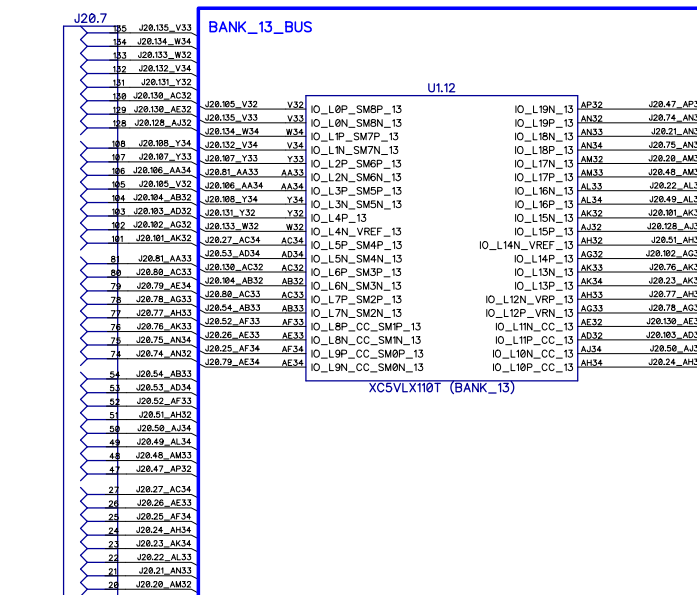
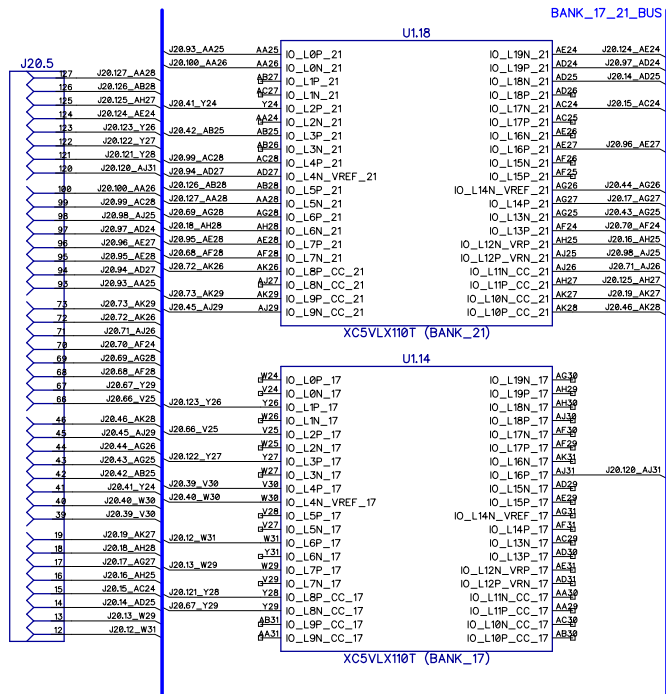
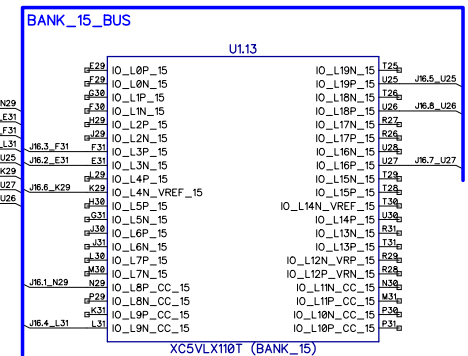
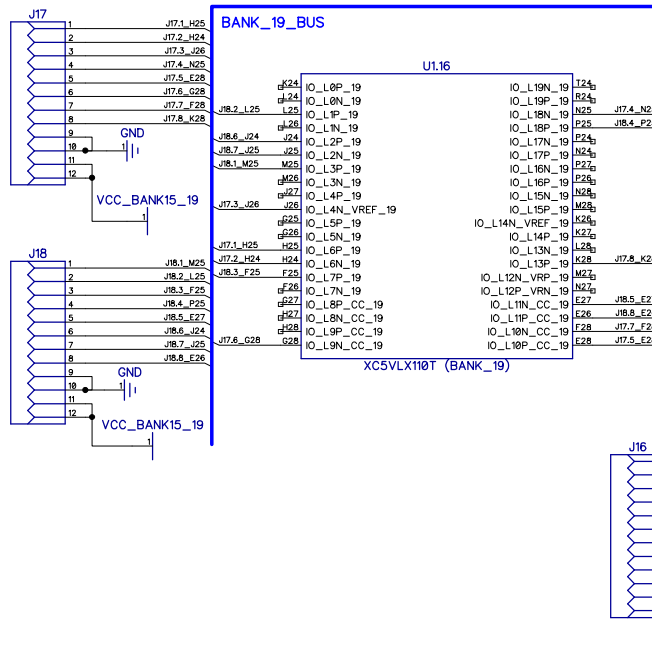
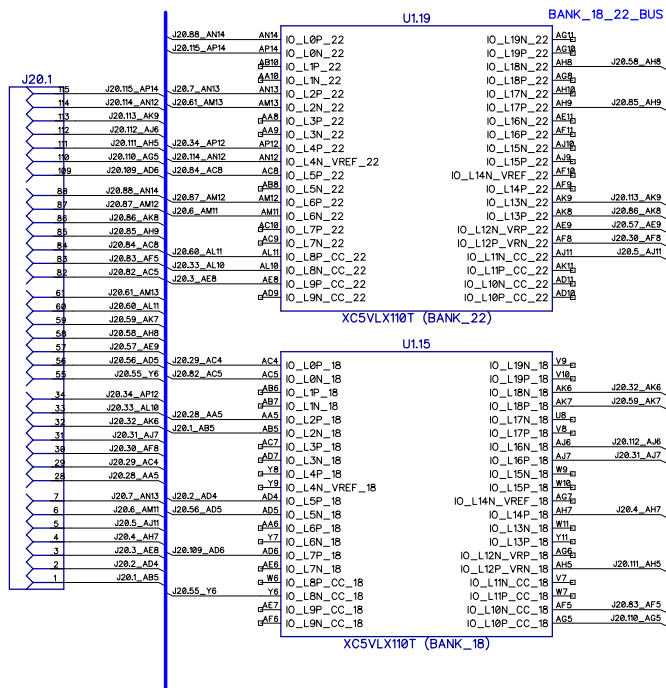
MODEL: XMF5-110-64-512 50/75M Rev.B



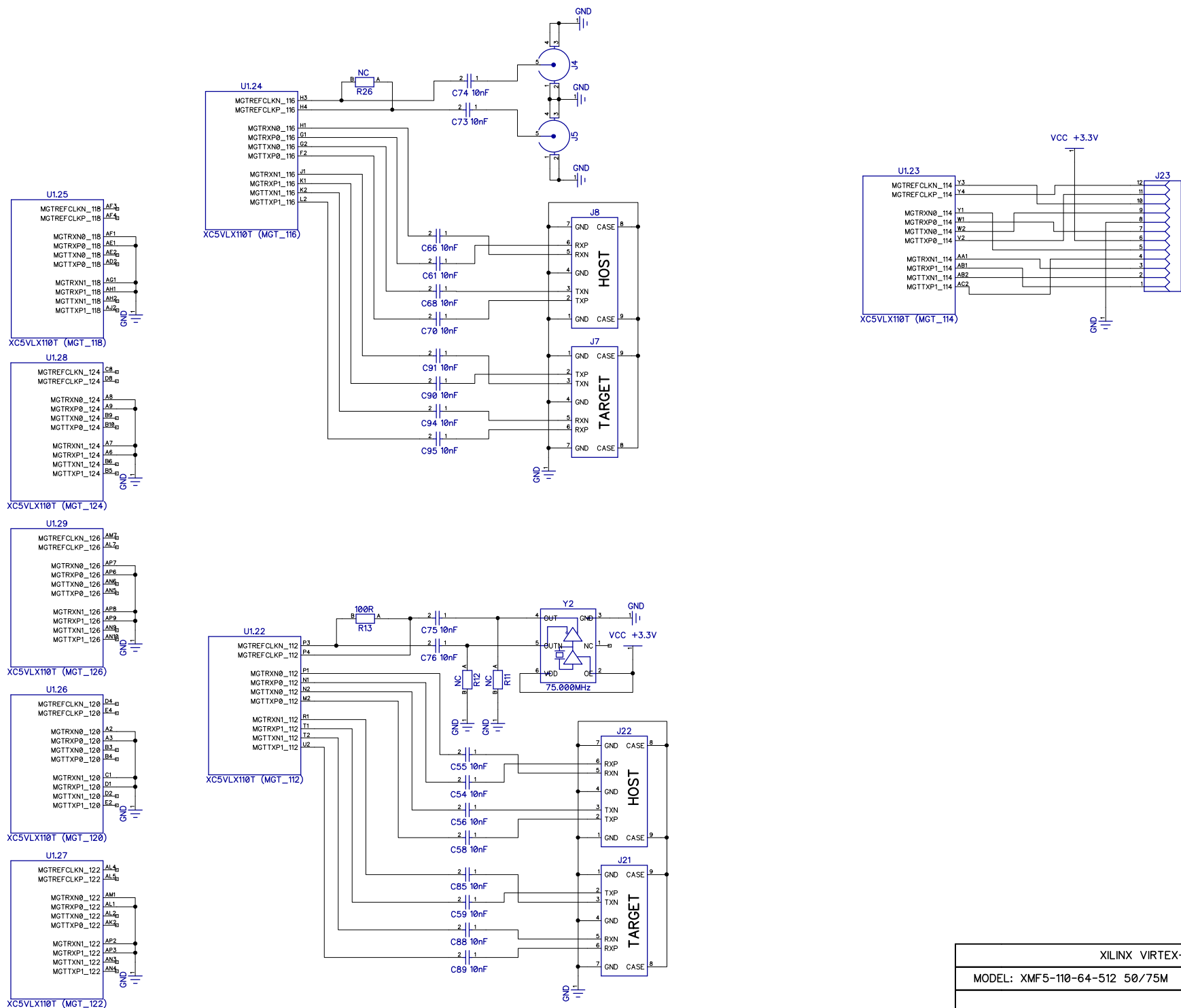




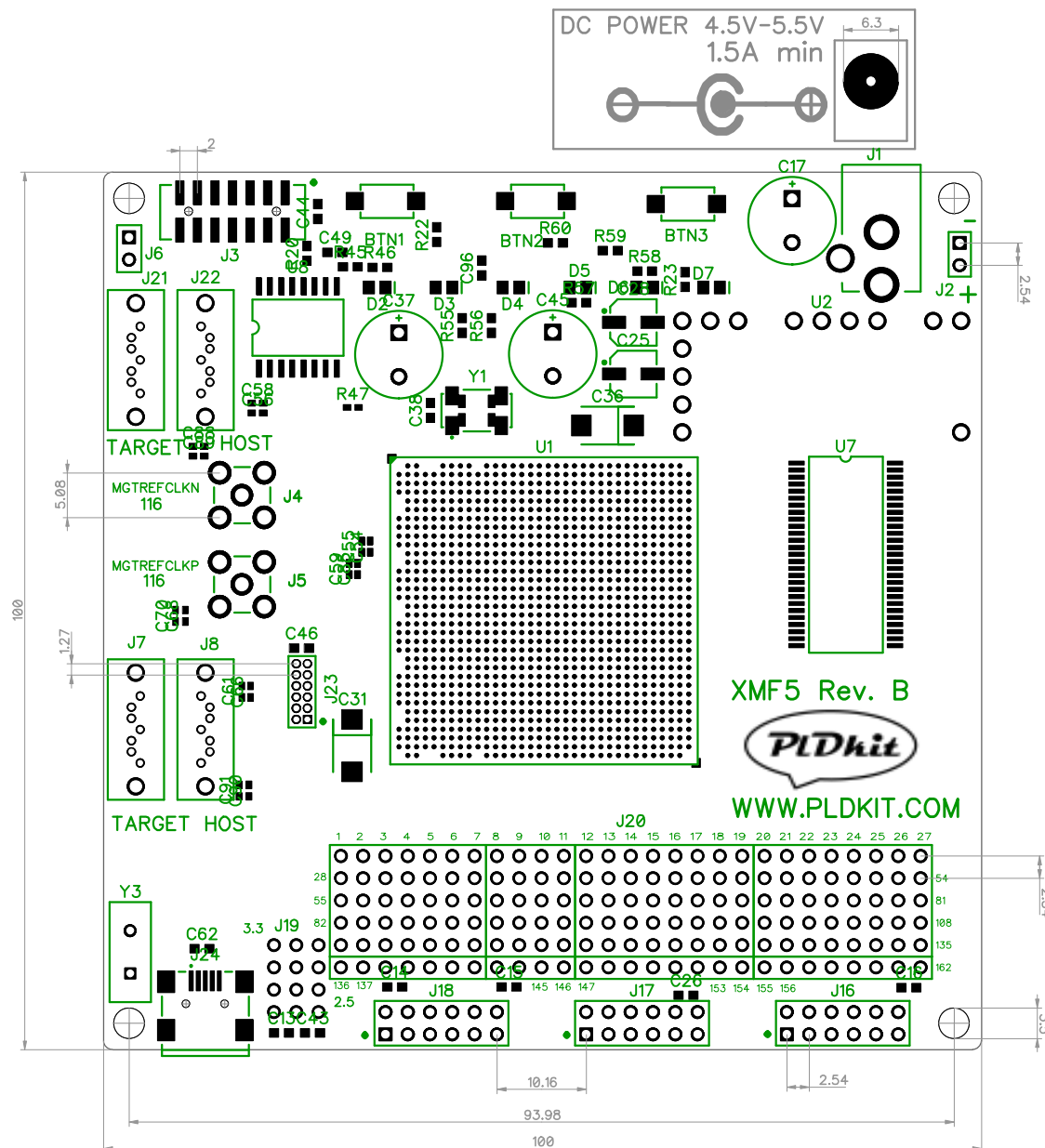




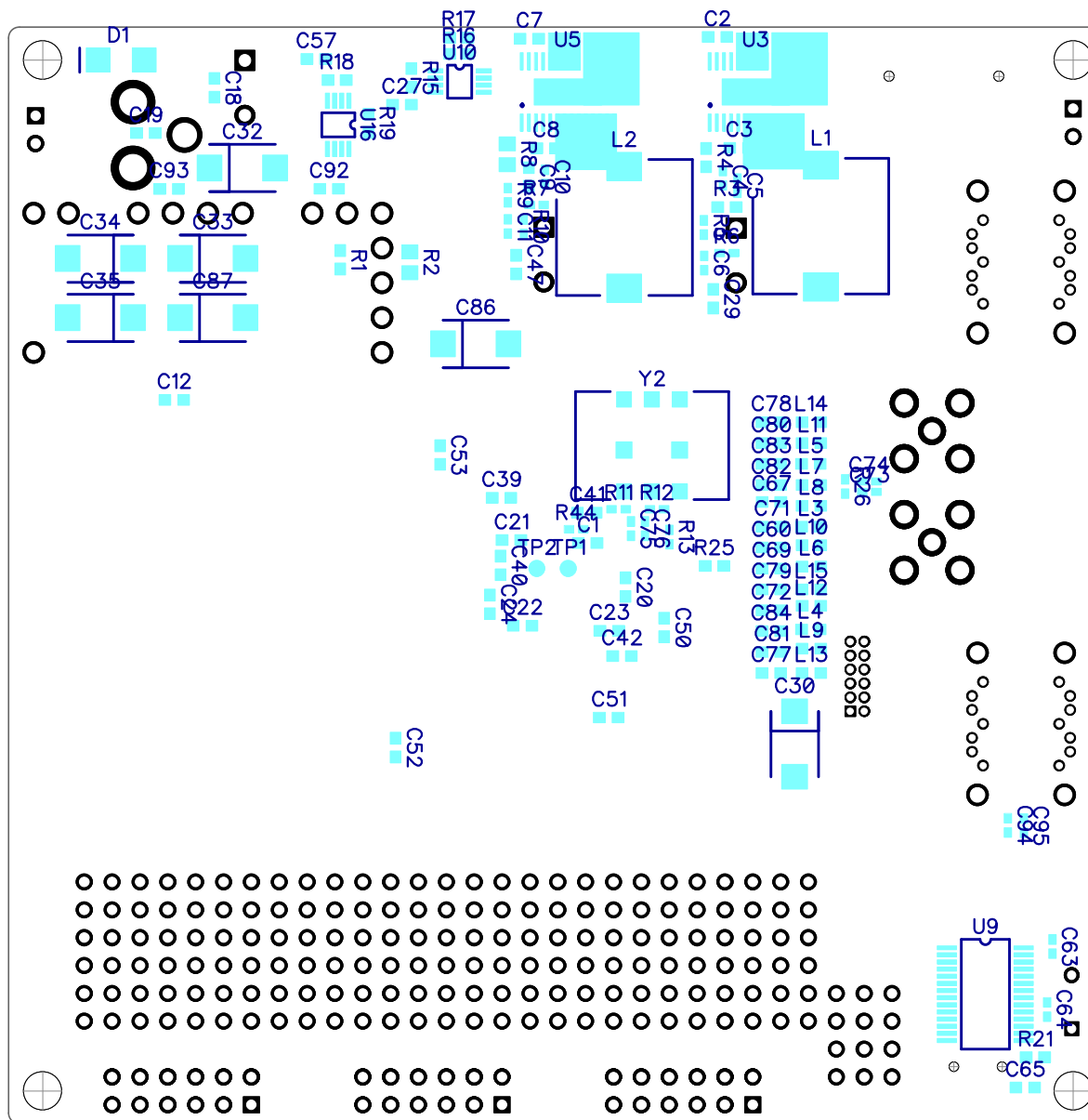
XILINX VIRTEX-5 FPGA MODULE			
MODEL: XMF5-110-64-512 50/75M	Rev. B	20.04.2015	Sheet 4/5
IO CONNECTORS			PLDkit OU <a href="http://www.pldkit.com">www.pldkit.com</a>



XILINX VIRTEX-5 FPGA MODULE			
MODEL: XMF5-110-64-512 50/75M	Rev. B	20.04.2015	Sheet 5/5
TRANSCIEVERS			PLDkit OU www.pldkit.com

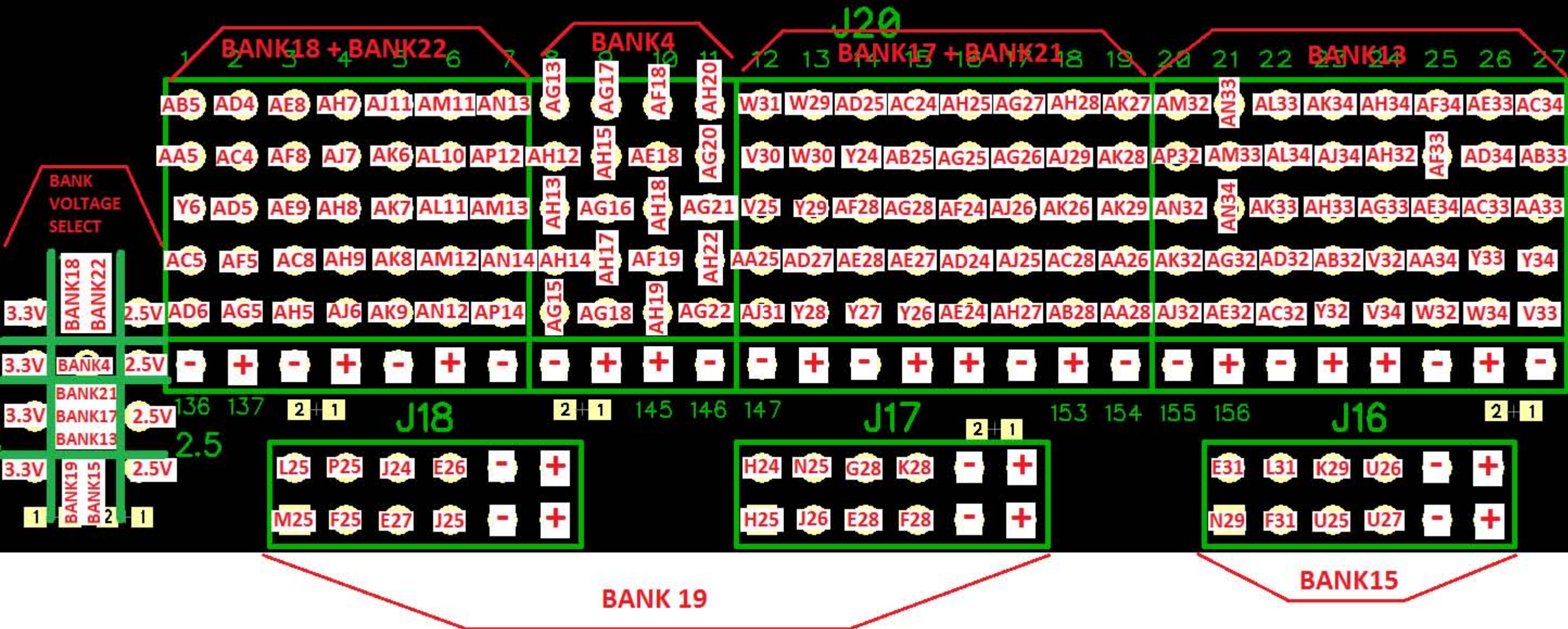


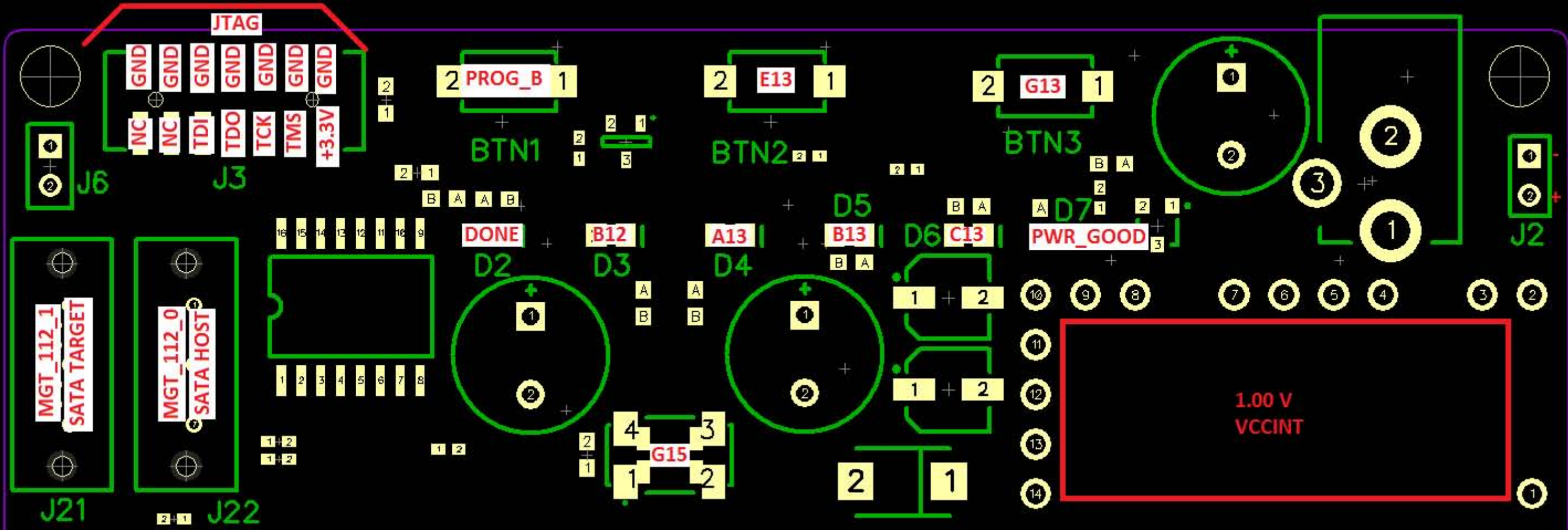




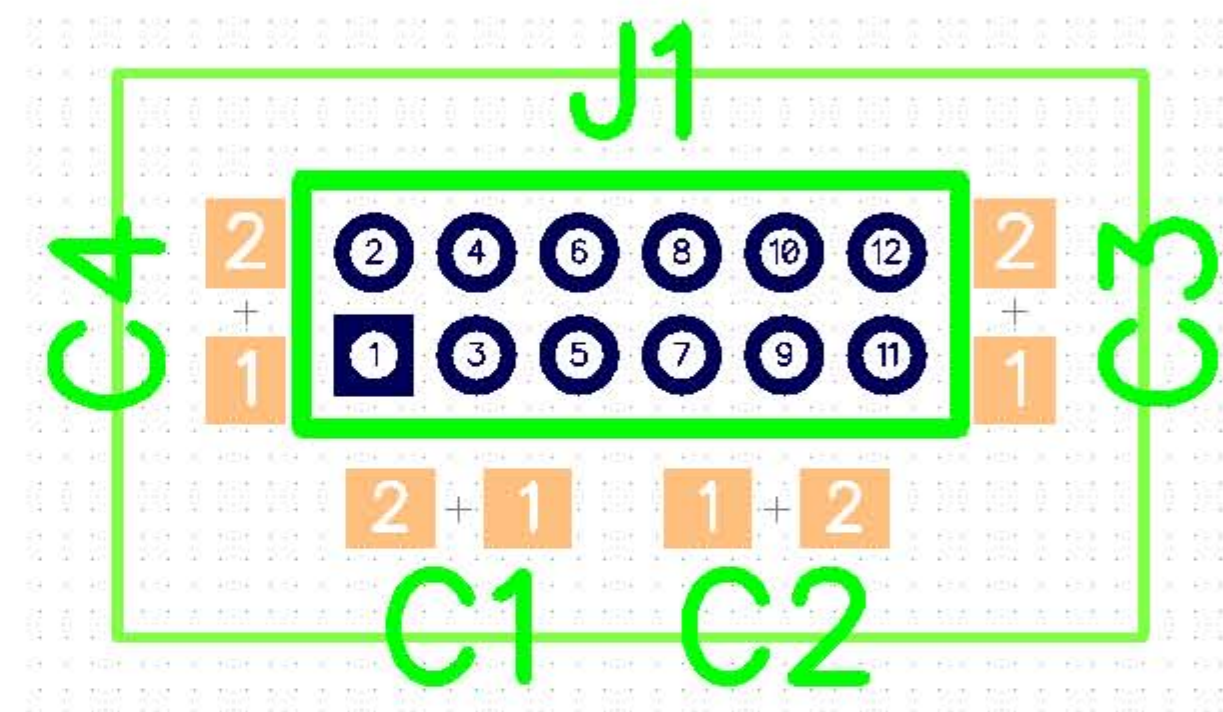
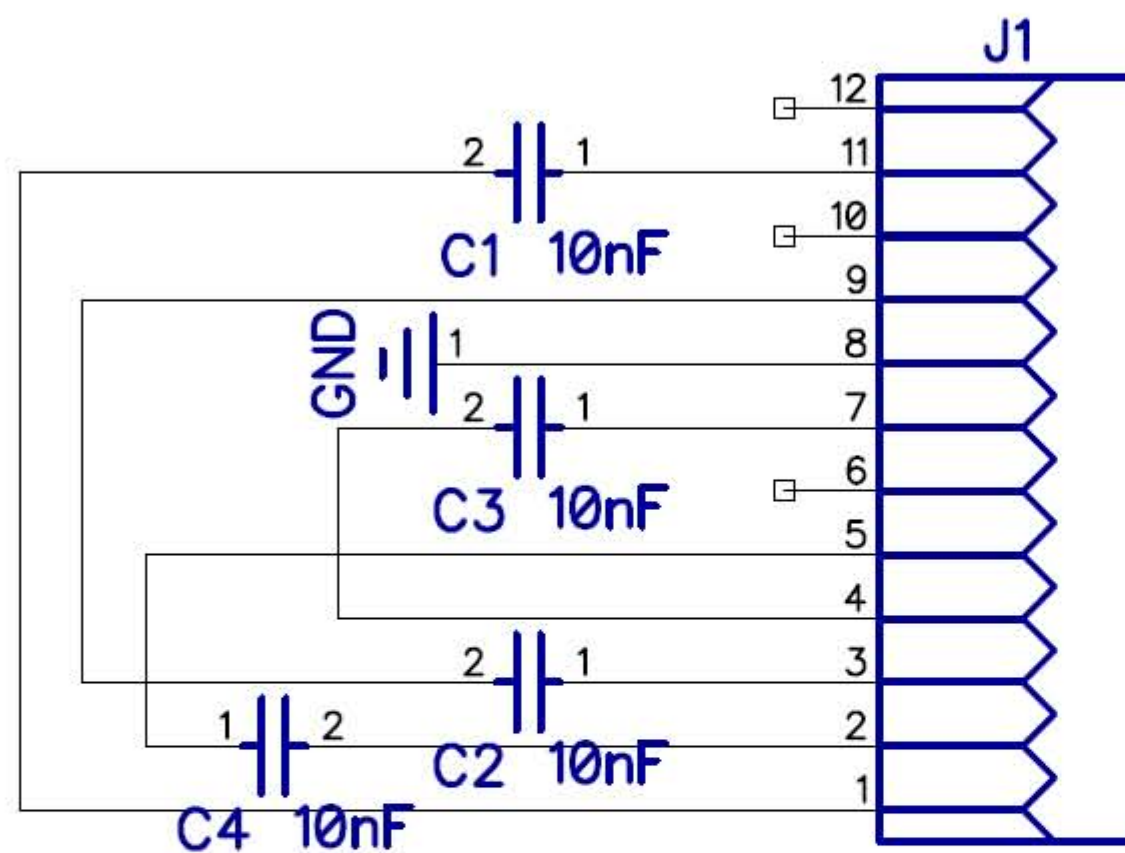
XILINX VIRTEX-5 FPGA MODULE			
MODEL: XMF5	Rev. B	19.04.2015	Sheet 1/1
PCB LAYOUT			PLDkit OU www.pldkit.com











# J23 GTP LOOP TEST JUMPER FOR XMF5

Rev. A

10.01.2014

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