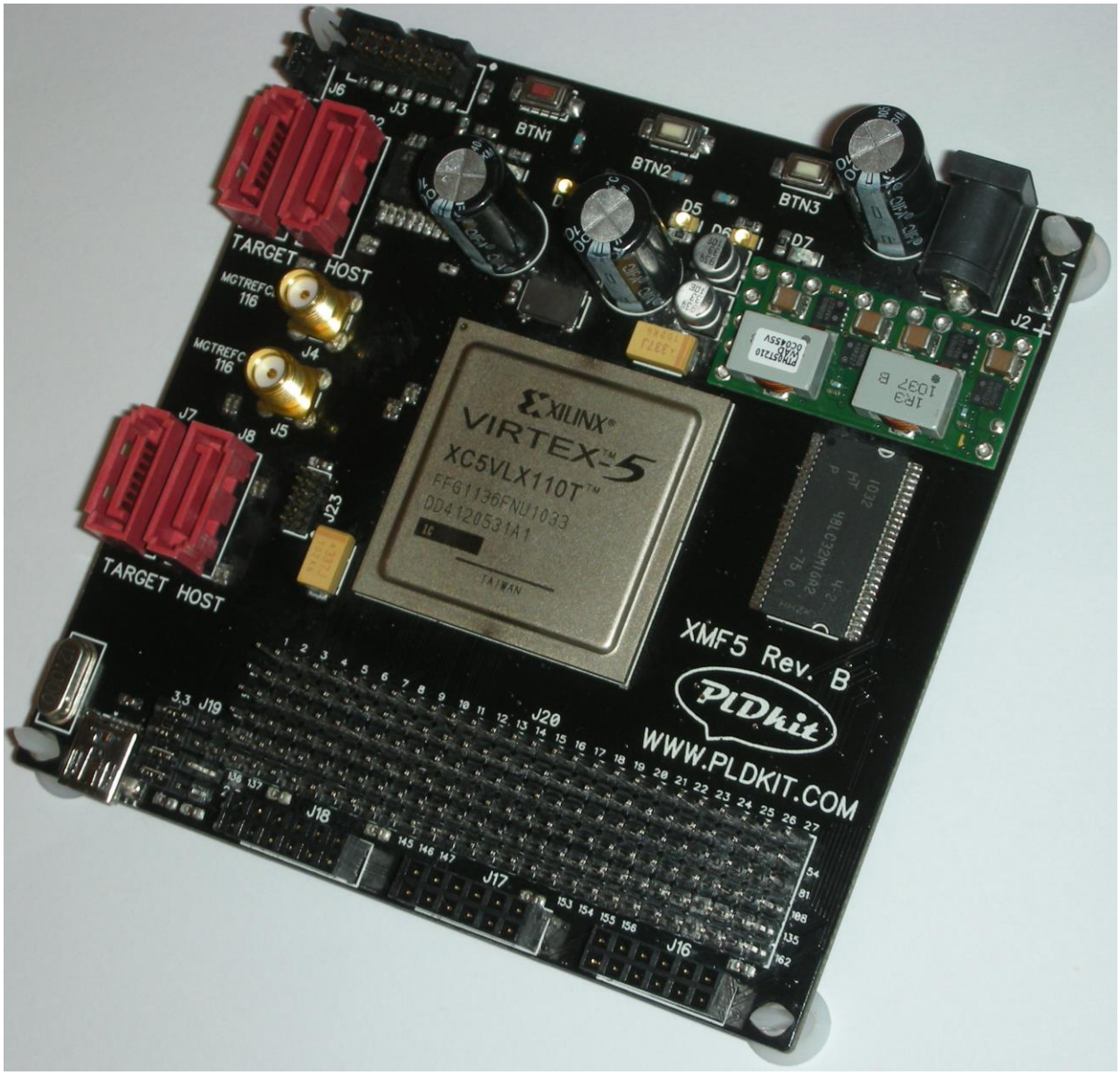
XILINX VIRTEX-5 FPGA MODULE USER's GUIDE

MODEL: XMF5-110-64-512 50/75M Revision B



Introduction

Xilinx Virtex-5 XMF5 FPGA module is a powerful and easy to use tool. Designed for rapid prototyping and implementing FPGA designs. Module can be used for educational purposes. Module can work independently, or as control module in the bigger design.

Features

1) XILINX XC5VLX110T FFG1136 1C FPGA
- 17280 Virtex-5 Slices (110592 Logic Cells)
- 64 DSP48E Slices
- 148x 36Kb RAM blocks (5328Kb, 550MHz)
- 6 Clock Management Tiles
- 1 Endpoint Block for PCI Express
- 4 Ethernet MACs
- 16 GTP RocketIO 3.75 Gb/s Transceivers (6 routed on this board)
- 680 User I/O (209 routed on this board)
- Fully supported by latest XILINX design tools

2) ST M25P64 SPI Flash
- 64Mbit
- SPI Bus Interface
- FPGA configuration
- Post-configuration access
- More than 100000 Program/Erase Cycles and 20 year data retention
- Fully supported by latest XILINX design tools

3) MICRON 48LC32M16A2 -75 SDRAM
- 512Mbit
- 133MHz

4) PL-2303 USB UART port

5) RocketIO Transceivers
- 2x SATA HOST port
- 2x SATA TARGET port
- One MGT clock input routed to SMA connectors
- Two transceivers routed to 1.27mm male header

6) Crystal oscillators
- 50MHz CMOS for IO
- 75MHz LVDS for Rocket IO

7) Four IO LEDs

8) Two IO push buttons

9) JTAG header
- FPGA
- Indirect Programming of SPI Serial Flash

10) Mode select jumper
- JTAG
- FLASH

11) Push button for manual initiation of configuration process

12) Reset supervision by power IC

13) Onboard power supply
- 3.3V 6A (IO, PERIPHERALS)
- 2.5V 6A (VCCAUX, IO)
- 1V 30A (CORE VOLTAGE)
- 1V 1.5A (Rocket IO)
- 1.2V 1.5A (Rocket IO)
- Input voltage range 4.5V – 5.5V

14) POWER-ON LED

15) DONE LED

16) 159 independent I/O routed to the connectors
- 6x27 male pin array (135 IO, 14 GND, 13 VCC)
- Three 2x6 female connectors (24 IO, 6 GND, 6 VCC)
- Peripheral modules support
- 2.54mm pitch for all connectors
- Selectable IO voltage: 3.3V or 2.5V

17) Small 100x100mm PCB

Instructions

1) The Virtex-5 family provides the newest most powerful features in the FPGA market. In addition to the most advanced, high-performance logic fabric, Virtex-5 FPGAs contain many hard-IP system level blocks. These features allow advanced logic designers to build the highest levels of performance and functionality into their FPGA-based systems. Built on a 65-nm state-of-the-art copper process technology, Virtex-5 FPGAs are a programmable alternative to custom ASIC technology. This particular board has XC5VLX110T FFG1136 1C FPGA (1136 ball package, speed grade 1, commercial temperature range 0°C to +85°C.

- Virtex-5 Family Overview:
  http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf
- Virtex-5 FPGA DC and Switching Characteristics:
  http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf
- Virtex-5 FPGA User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug190.pdf
- Virtex-5 FPGA Configuration User Guide:
  http://www.xilinx.com/support/documentation/user_guides/ug191.pdf
- Virtex-5 FPGA XtremeDSP Design Considerations:
  http://www.xilinx.com/support/documentation/user_guides/ug193.pdf

2) U8 is M25P64 64Mb ST SPI flash IC. 64Mb is more than required for XC5VLX110T single bitstream. This allows storing of multiple bitstreams in the flash. Also, after FPGA is configured, free space can be used by embedded processor. “led_RAM_UART” demo design will be stored in flash, to test some of the module functions. Because SPI is a serial interface, and bitstream for XC5VLX110T is quite big, it is taking 14 seconds to load bitstream, after board is powered on.

- M25P64 datasheet:
  http://pldkit.com/download/M25P64.pdf
- Post-Configuration Access to SPI Flash Memory with Virtex-5 FPGAs:
  http://www.xilinx.com/support/documentation/application_notes/xapp1020.pdf

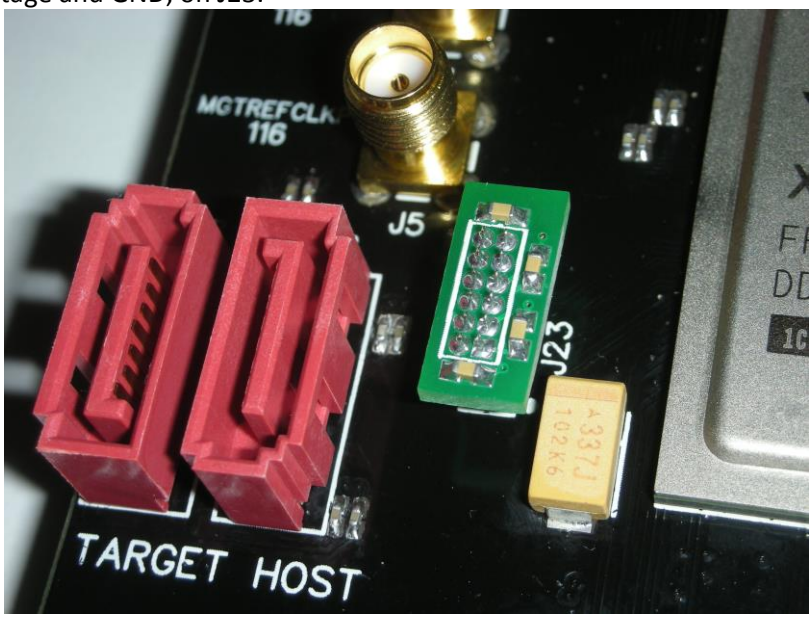
3) U7 is MICRON 48LC32M16A2 -75 512Mbit SDRAM with maximum frequency of 133MHz. When factory demo design is loaded to FPGA, Microblaze soft processor will run memory test. Results

of the test can be seen in UART console. Pressing BTN2 together with BTN3 will reset Microblaze.

- 48LC32M16A2 -75 datasheet: http://pldkit.com/download/48LC32M16A2.pdf
- LogiCORE IP Multi-Port Memory Controller: http://www.xilinx.com/support/documentation/ip_documentation/mpmc/v6_05_a/mpmc.pdf

4) Board has PL-2303 USB UART port. J24 is mini-USB connector, located at the bottom left corner of the board. TX is connected to AG12, RX is connected to AF16. When factory demo design is loaded to FPGA, UART is controlled by Microblaze soft processor. It is possible to see RAM test results from console, after board is powered on. Use these settings to establish UART connection: 9600-8-n-1.

5) Board has 3 GTP_DUAL tiles routed, which gives 6 GTP RocketIO Transceivers. There is 75MHz LVDS oscillator and two SATA ports, connected to MGT_112 tile. Any of onboard transceivers can be clocked from this 75MHz LVDS oscillator. Transceivers also can be clocked from FPGA internal clock. J22 and J8 are SATA HOST ports. Peripherals like SATA hard drive, can be connected there. J21 and J7 are SATA TARGET ports. External SATA controller can be connected there, and XMF5 will act as SATA peripheral. You can still use TARGET port as HOST, or HOST port as TARGET, if connect SATA crossover cable, instead of ordinary. There are two SMA connectors and two SATA ports, connected to MGT_116 tile. External differential clock signal can be connected to J4 and J5. Place termination resistor R26, if needed. Both transceivers of MGT_114, including MGTREFCLK pins, are routed to J23, 1.27mm pitch male connector. J23 also has GND and VCC 3.3V pins. Additional modules, like Ethernet PHY can be connected, and powered, from J23. When “loop_test_GTP” demo design is loaded to FPGA, transceivers can be tested, by looping one to another. To test MGT_112, connect J22 to J21 with SATA cable. LED D5 will turn on, if test is passed. To test MGT_116, connect J8 to J7 with SATA cable. LED D6 will turn on, if test is passed. To test MGT_114, connect included, 12-pin loop test jumper, to J23. LED D4 will turn on, if test is passed. Be careful, when connecting J23 loop, it must be connected with correct polarity. Connecting the loop wrongly can damage the transceivers, because there is 3.3V voltage and GND, on J23.



“loop_test_GTP” demo design includes Chipscope core. To use it, load design, and connect to FPGA with Chipscope Pro Analyzer 14.1.

- Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide: http://www.xilinx.com/support/documentation/user_guides/ug194.pdf
- Virtex-5 FPGA RocketIO GTP Transceiver User Guide: http://www.xilinx.com/support/documentation/user_guides/ug196.pdf
- LogiCORE IP Virtex-5 FPGA RocketIO GTP Transceiver Wizard v2.1: http://www.xilinx.com/support/documentation/ip_documentation/v5_gtpwizard_ds590.pdf
- LogiCORE™ IP Virtex®-5 FPGA RocketIO™ GTP Transceiver Wizard v2.1 Getting Started Guide: http://www.xilinx.com/support/documentation/ip_documentation/v5_gtpwizard_gsg188.pdf
- Serial ATA Physical Link Initialization with the GTP Transceiver of Virtex-5 LXT FPGAs: http://www.xilinx.com/support/documentation/application_notes/xapp870.pdf

6) 50MHz CMOS crystal oscillator is connected to pin G15. 75MHz LVDS crystal oscillator is connected to MGT_112 tile. You can use DCM to divide or multiply clock frequency. Additional clock signals can be connected from outside.

7) There are 4 LEDs connected to FPGA IO. Pins B12, A13, B13 and C13.

8) There are two momentary push buttons, with pull up resistors, connected to FPGA IO. Pins G13 and E13.

9) J3 is JTAG connector. Only FPGA IC is connected straight to J3. To program SPI flash, indirect SPI flash programming method should be used. 25P64 SPI flash is supported by iMPACT 14.1.

- Configuring Xilinx FPGAs with SPI Serial Flash: http://www.xilinx.com/support/documentation/application_notes/xapp951.pdf

10) J6 is FPGA mode select jumper. When jumper is connected, master SPI mode is selected (M[2:0] = <0:0:1>). In this mode, FPGA is loading configuration from SPI flash. When Jumper is removed, JTAG mode is selected (M[2:0] = <1:0:1>). Make sure, that during flash indirect programming jumper is installed. Otherwise, you may get error “DONE pin did not go high”.

11) There is push button BTN1 connected to PROGRAM_B pin for manual initiation of configuration process at any time. To configure or reconfigure FPGA from FLASH, insert J6 jumper and press PROG_B button. To clear FPGA configuration and put it in JTAG mode – remove J6 jumper and press PROG_B button.

12) PWRGD pin of U3 TPS54610 power regulator is connected to PROGRAM_B pin. PWRGD pin of U5 TPS54610 power regulator is connected to SS/ENA pin of U3. Because of this, power regulators are sequenced, and PROGRAM_B signal is asserted low whenever 2.5v or 3.3v voltage is not in power-good range. This scheme also ensures that during power on, flash will be ready before FPGA, for proper bitstream loading.

13) Board has powerful power supply, to serve the needs of VIRTEX-5 FPGA. Core voltage for FPGA is provided by PTH05T210W. Together with 2970uF tantalum capacitors and TurboTrans™ Technology, it is very stable, accurate and powerful solution. PTH05T210W can deliver up to 30A current for FPGA core. 3.3V and 2.5V supplies are built with two 6A DC-DC converters. 3.3V is used by board peripherals and by FPGA IO banks. 2.5V is used for FPGA VCCAUX and also can be used to supply FPGA IO banks. Supply voltage for banks 18,22,4,21,17,13,19,15 can be selected between 3.3V and 2.5V, with J19 jumpers. If some of these banks will have huge load, it is recommended to replace jumpers with solder bridges, to achieve better current flow. There are

two voltage regulators to produce 1.2V and 1V for FPGA GTP transceivers. Input power supply must be within range of 4.5V to 5.5V. It must provide at least 1.5A current. Much bigger current may be required, for your custom FPGA design. J1 DC jack can be used to connect DC power adapter. Also two-pin header J2 can be used, to provide power for low load designs. Be careful with voltage polarity. There is protective diode D1 on the input, to protect from wrong polarity and overvoltage. But it has limited abilities. Please don't touch powered DC-DC converters with naked fingers, to check temperature, or something else. This can lead to converter instability and permanent damage. You can use IR thermometer, to safely measure temperature.

14) D7 is a POWER-ON LED. When it is on, it means that there is input DC voltage connected.

15) D2 is a DONE LED. It turns on after FPGA has finished configuration process.

16) There are total 159 I/O pins, what are routed to the connectors, and can be used in your design. Please refer to the board schematics, to get information about connections. All I/O are independent and not crossing with any module peripherals. J20 is 162 male pin array. By columns, it is divided to four groups: 1 to 7 column - BANK18 + BANK22, 8 to 11 column - BANK4, 12 to 19 column - BANK17 + BANK21, 20 to 27 column - BANK13. By rows, it is divided to two parts: row 1 to 5 are IO pins, row number 6 is power pins. J16, J17 and J18 are 6x2 female connectors. J18 and J17 routed to BANK19, J16 to BANK15. Each connector has 8 IO, 2 VCC and 2 GND. These female connectors are designed specially to support peripheral modules. Peripheral modules, with compatible male connectors, can be ordered from PLDkit web site, or from some other suppliers. Supply voltage for banks can be set separately with J19 jumpers, 3.3V or 2.5V. Please note that HSWAPEN FPGA pin is connected to GND, this means that when FPGA is not configured, all IO pull-up resistors are enabled. When "io_test" demo design is loaded to FPGA, IO connectors can be tested. Use fly wire, to connect IO pins one by one to BANK VCC. Test is passed if LEDs were turning on, every time when one of IO pins is connected to VCC. If there is missing contact or short circuit between IO - LEDs will not turn on. Be careful, and don't make short circuit between VCC and GND. Also don't connect main 5v voltage to IO pins.

17) Board size is quite small – 100mm x 100mm. It can be easily mounted inside of some other device. With some designs, FPGA can heat quite fast. Adhesive heatsink can be mounted on top of FPGA. Internal FPGA thermal diode is routed to test points TP2 (DXP_0) and TP1 (DXN_0). By connecting this diode to an external signal conditioning IC (thermal monitor), the die temperature could be determined. FPGA system monitor is disabled on this board.

- Virtex-5 FPGA System Monitor User Guide: http://www.xilinx.com/support/documentation/user_guides/ug192.pdf

Powering up the board for the first time

1) Connect 5V 2A to J1, with correct polarity.
2) Demo design will be automatically loaded into FPGA from the Flash, if jumper J6 is not removed. Loading will take 14 seconds.
3) LEDs D3-D6 will start blinking. This process can be adjusted with buttons BTN2 and BTN3.
4) Connect micro-USB to the J24. Set terminal settings to 9600-8-n-1.
5) Reset Microblaze soft processor, by pressing BTN2 together with BTN3.
6) Results of the SDRAM test will be sent to UART.