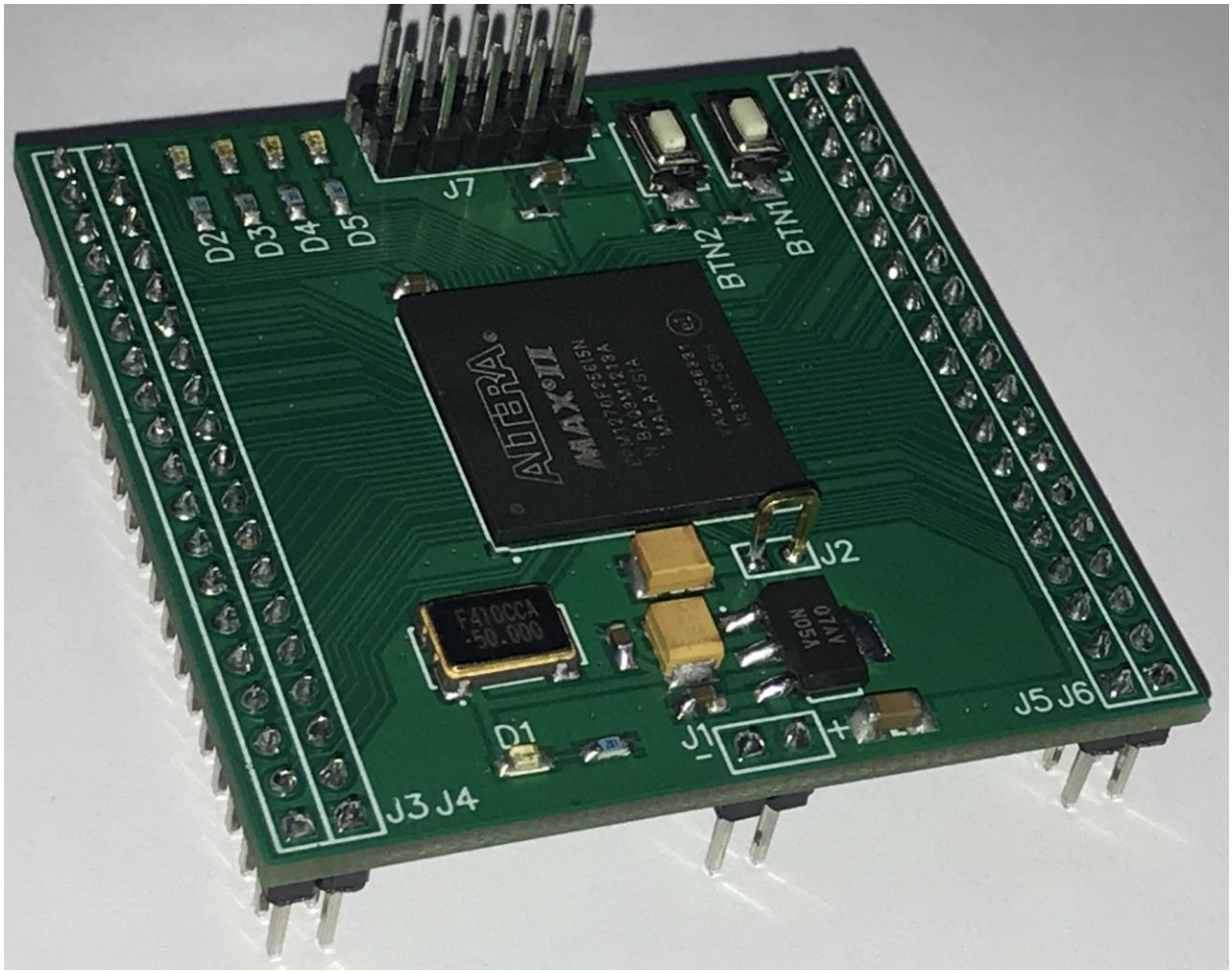
# ALTERA MAX-II CPLD MODULE USER's GUIDE

***MODEL: AM3C2  Revision A***



# Introduction

**ALTERA MAX-II AM3C2 CPLD module is a low cost and easy to use tool. Designed for rapid prototyping and implementing CPLD designs. This module can be used independently, for education, or can be used as core module, for a bigger design.**

# Features

**1)** ALTERA EPM1270 F256 I5 CPLD
- 1270 LEs (570 to 1270 Equivalent macrocell range)
- Instant-on, non-volatile architecture
- Provides four global clocks with two clocks available per logic array block (LAB)
- UFM block up to 8 Kbits for non-volatile storage
- Bus-friendly architecture including programmable slew rate, drive strength, bus-hold, and programmable pull-up resistors
- Supports hot-socketing
- 304 MHz fCNT

**2)** Onboard IO peripherals
- 4 LEDs
- 2 push buttons
- 50 MHz CMOS crystal oscillator

**3)** Handy configuration
- Onboard JTAG header

**4)** Onboard power supply
- Input voltage range 5V – 15V
- 3.3V LDO
- POWER-ON LED
- J2 jumper to use external I/O voltage 1.5V-3.3V

**5)** 72 independent I/O routed to the connectors
- Four 1x19 male connectors (18 IO, 1 VCC or 1 GND)
- 2.54mm pitch for all connectors
- 1.5V-3.3V External I/O voltage can be used
- Small 50x50mm PCB designed to fit on the prototyping board with 2.54mm pitch

# Instructions

**1)** This board has EPM1270 F256 I5 CPLD (256 ball package, speed grade 5, industrial temperature range -40°C to +100°C). The MAX® II family of instant-on, non-volatile CPLDs is based on a 0.18-µm, 6-layer-metal-flash process, with densities from 240 to 2,210 logic elements (LEs) (128 to 2,210 equivalent macrocells) and non-volatile storage of 8 Kbits. MAX II devices offer high I/O counts, fast performance, and reliable fitting versus other CPLD architectures. Featuring MultiVolt core, a user flash memory (UFM) block, and enhanced in-system programmability (ISP), MAX II devices are designed to reduce cost and power while providing programmable solutions for applications such as bus bridging, I/O expansion, power-on reset (POR) and sequencing control, and device configuration control.

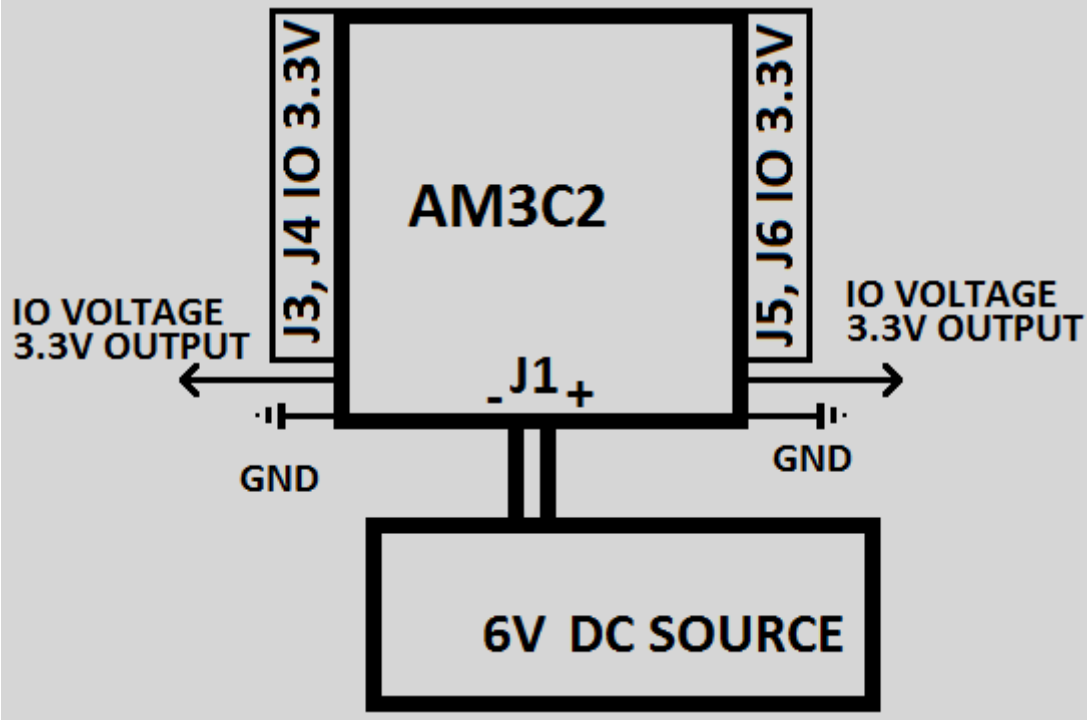
- MAX II Device Handbook: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/max2_mii5v1.pdf
- Dedicated Pin Information for the MAX® II EPM1270: https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/dp/max2/epm1270.pdf

**2)** Board has few simple peripherals onboard: 4 yellow LEDs, 2 momentary active-low push buttons with pull up resistors. AM3C2 module is equipped with 50 MHz CMOS oscillator, what is connected to pin H5.

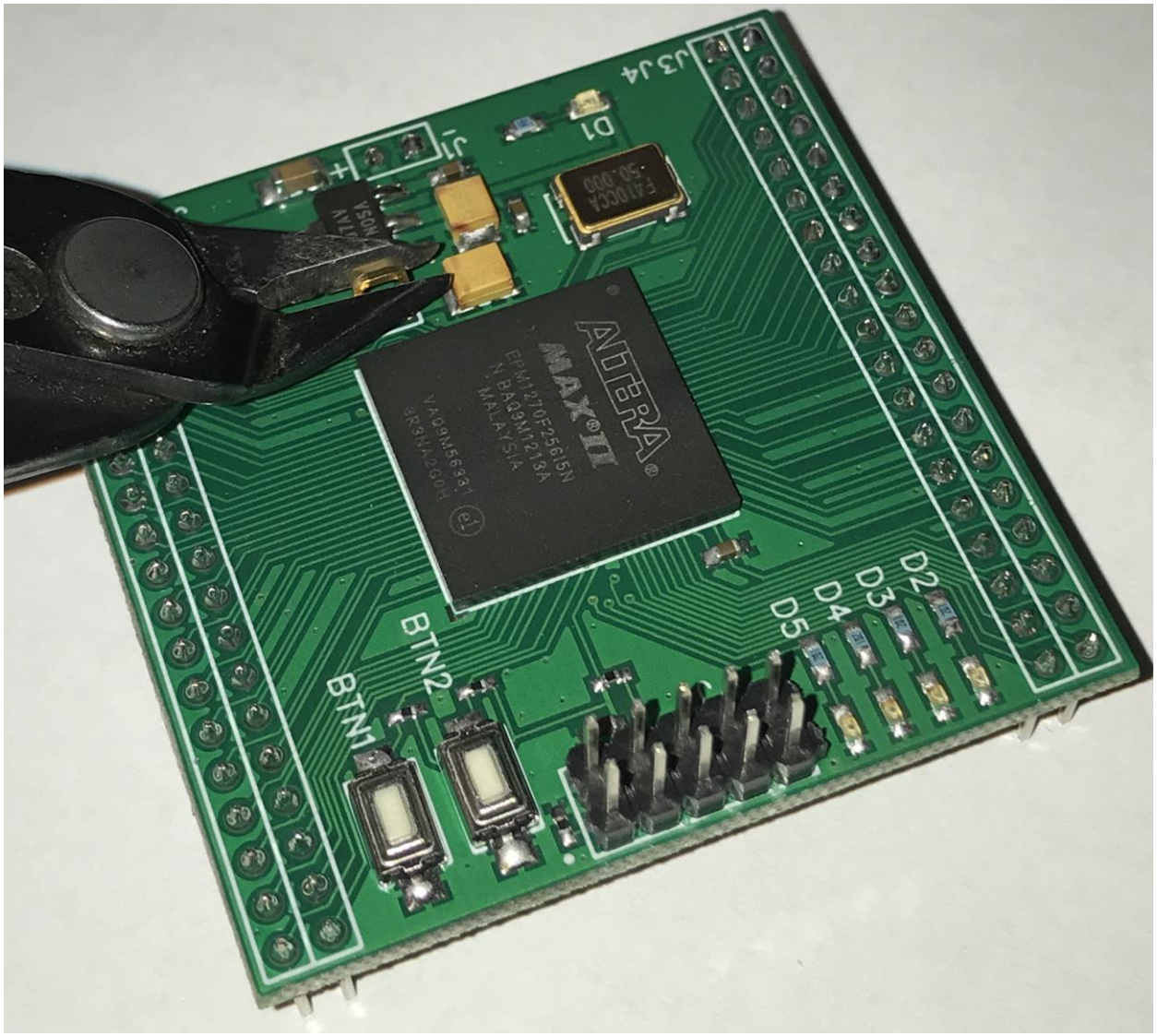
**3)** J7 is JTAG header, with 2.54mm pitch. Use JTAG-USB or JTAG-LPT cable, to program CPLD. JTAG signals have 3.3V voltage levels.

**4)** AM3C2 module has one 3.3V LDO onboard. By default, 3.3V is used as core voltage, by board peripherals, and by CPLD IO. When J2 jumper is intact, 3.3V is delivered to CPLD, to J3, and J5. If J2 is cut away, then, external IO voltage should be connected to J3-1 or J5-1. Allowed IO voltage range is -0.5V to 4.0V. If voltage limit is breached, the CPLD IC will be permanently damaged.

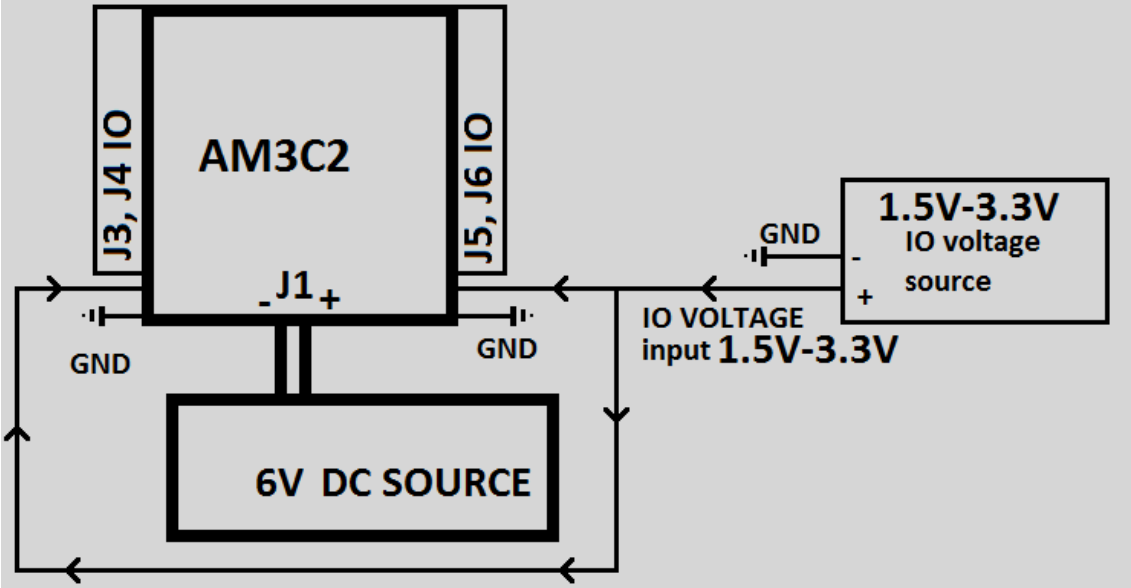
Default IO voltage configuration:



If you need to use XM3C2 with IO voltage, what is not 3.3 volt, then cut J2:



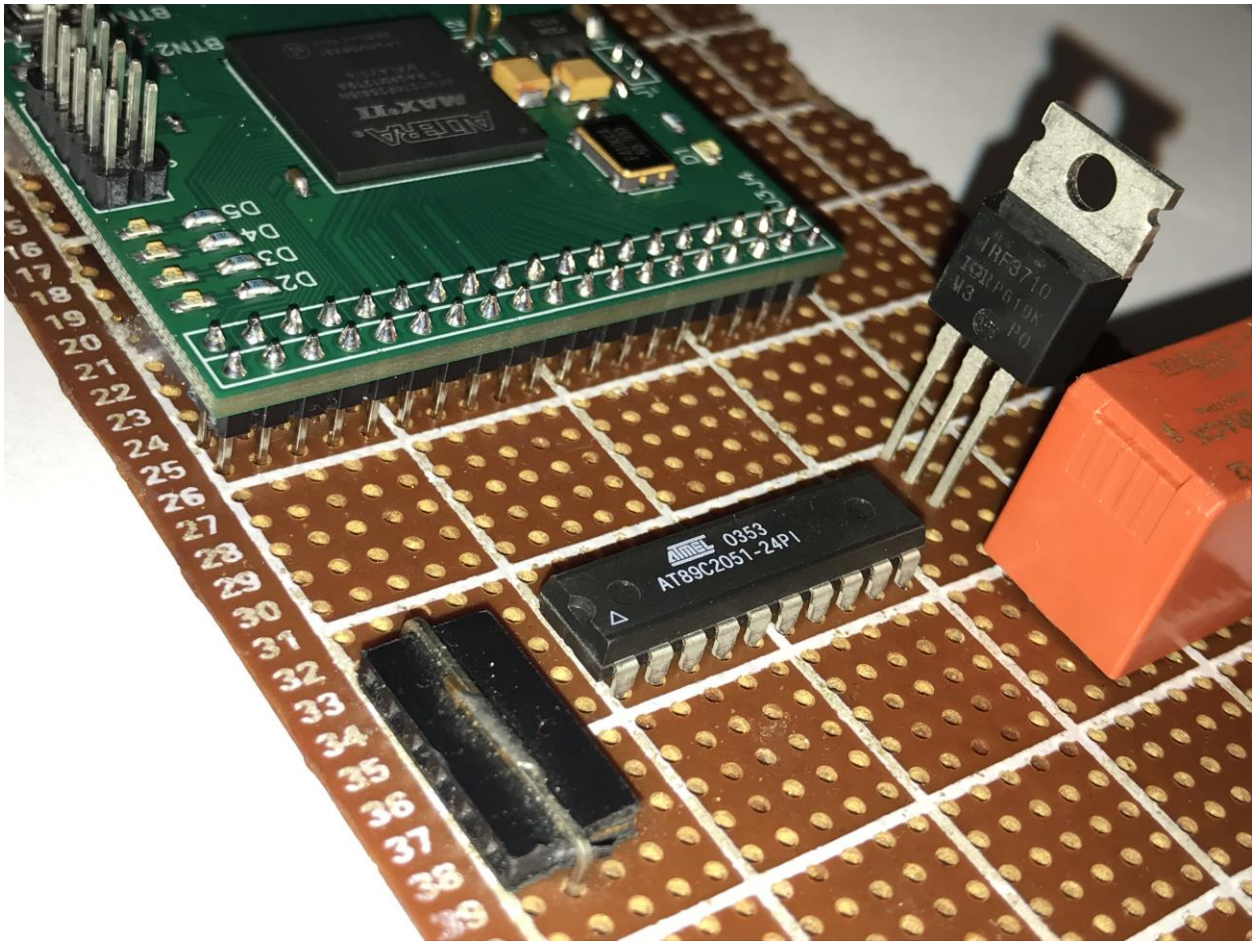
Connect external IO voltage 1.5V-3.3V, to J3 pin 1, or J5 pin 1:




D1 is a POWER-ON LED, when it lit - it means that there is input DC voltage connected. Input voltage range is 5V to 15V. Voltage, what is higher than 15V, can damage the board.

**5)** There are total 72 I/O pins, what are routed to the connectors, and can be used in your design. Please refer to the board schematics, to get information about connections. All I/O are independent and not crossing with any boards peripherals. J3, J4, J5 and J6 are 19x1 male connectors. Each connector has 18 IO, 1 VCC or 1 GND. Zip archive, for this board, contains QUARTUS project. It is test demo, what is programmed to CPLD during manufacturing. When board is powered on, with programmed demo project, LEDs will blink. Blinking can be adjusted with buttons. Use fly wire, to connect IO pins one by one to GND. All LEDs will turn on, every time when one of IO pins is connected to GND. If there is missing contact or short circuit between IO, LEDs will be blinking. Be careful, and don't make short circuit between VCC and GND.

Module size is quite small and it is designed to fit perfectly on 2.54mm pitch prototype board.




# Powering up the board for the first time

1) Connect 5v to J1, with correct polarity. Red LED D1 should turn on.
2) Demo design will be automatically loaded by CPLD.
3) IO LEDs will start blinking. This process can be adjusted with buttons, or by connecting one of the I/O pins to GND.
4) Use ALTERA (INTEL) QUARTUS design suite, to create and compile your project.
5) Use ALTERA (INTEL) QUARTUS, and compatible JTAG cable, to upload compiled project into CPLD. You can also use JTAG cables what are not supported by “QUARTUS”, with third party software.