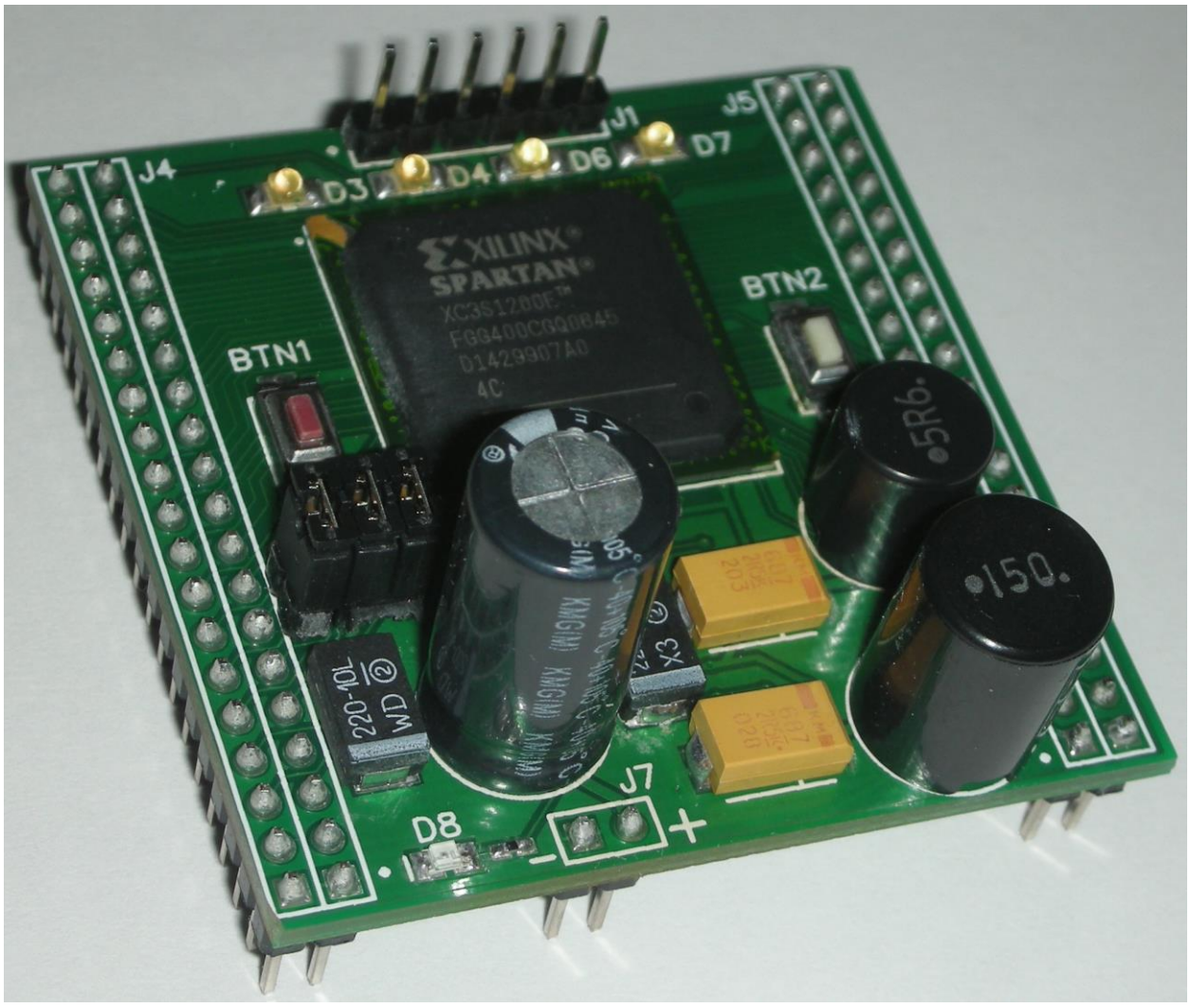
XILINX SPARTAN-3E FPGA MODULE USER's GUIDE

MODEL: XMF3E Revision A



Introduction

XILINX SPARTAN-3E XMF3E FPGA module is a low cost and easy to use tool. Designed for rapid prototyping and implementing FPGA designs. This module can be used independently, for education, or can be used as core module, for bigger design.

Features

1) XILINX XC3S1200E FGG400 4C FPGA
- 1200000 gates (19512 Logic Cells)
- 28x 18x18 hardware multipliers
- 28x 18K-bits block RAMs (504K)
- 8 Digital Clock Managers
- Fully supported by latest XILINX design tools

2) XILINX XCF08P FLASH
- 8 Mbit Platform Flash PROM
- IEEE Standard 1149.1/1532 Boundary-Scan (JTAG) support for programming
- Endurance of 20000 Program/Erase Cycles
- Fully supported by latest XILINX design tools

3) Reset supervision IC and reset push button

4) Onboard IO peripherals
- 4 LEDs
- 1 push button
- 50 MHz CMOS crystal oscillator

5) Handy configuration
- Onboard JTAG header
- Mode select jumper
- DONE LED

6) Onboard power supply
- Input voltage range 3.5V – 6.5V
- TPS75003, Triple-Supply Power Management IC for 3.3V, 2.5V and 1.2V
- 1.8V LDO
- POWER-ON LED

7) 76 independent I/O routed to the connectors
- Four 1x19 male connectors (18 IO, 1 VCC or 1 GND)
- 2.54mm pitch for all connectors
- 3.3V IO voltage
- Small 50x50mm PCB designed to fit on the prototyping board with 2.54mm pitch

Instructions

1) XILINX XC3S1200E is big FPGA, from SPARTAN-3E family. This particular board has XC3S1200E FGG400 4C FPGA (400 ball package, speed grade 4, commercial temperature range 0°C to +85°C).
- SPARTAN-3E FPGA family datasheet: http://www.xilinx.com/support/documentation/data_sheets/ds312.pdf
- User Guide: http://www.xilinx.com/support/documentation/user_guides/ug331.pdf

2) XILINX XCF08P is 8 Mbit platform Flash PROM with JTAG interface. There are 8,388,608 configuration bits in XCF08P Flash. Demo design will be stored to flash during manufacturing. With this demo, most of the boards functions can be tested.

- Platform flash PROM user guide:
  http://www.xilinx.com/support/documentation/user_guides/ug161.pdf

3) XMF3E FPGA module has MAX809 reset supervisor IC, connected to PROG_B pin. The function of the MAX809 is to monitor the 3.3v VCC supply voltage, and assert a PROG_B signal low whenever this voltage declines below the 3.08v reset threshold. The reset signal remains asserted for 240ms after VCC rises above the threshold. This ensures that during power on, flash will be ready before FPGA, for proper bitstream loading. Also, there is push button BTN1 connected to PROG_B pin for manual initiation of configuration process at any time.

4) Board has few simple peripherals onboard: 4 yellow LEDs (A7,A8,A13,A12), 1 momentary active-low push button with pull up resistor (M18). XMF3E module is equipped with 50 MHz CMOS oscillator, what is connected to pin A10.

5) J1 is JTAG header. There are two devices on JTAG chain: FPGA and Flash. D5 is FPGA DONE LED. It turns on after FPGA has finished configuration process. J2 connector is for selecting FPGA configuration mode. By default all jumpers on J2 will be installed. When powered, FPGA will load demo design from the flash. To set JTAG mode, remove M0 and M2 jumpers, leave jumper M1 on the board, and press PROG_B reset button.

- Configuration user guide:
  http://www.xilinx.com/support/documentation/user_guides/ug332.pdf

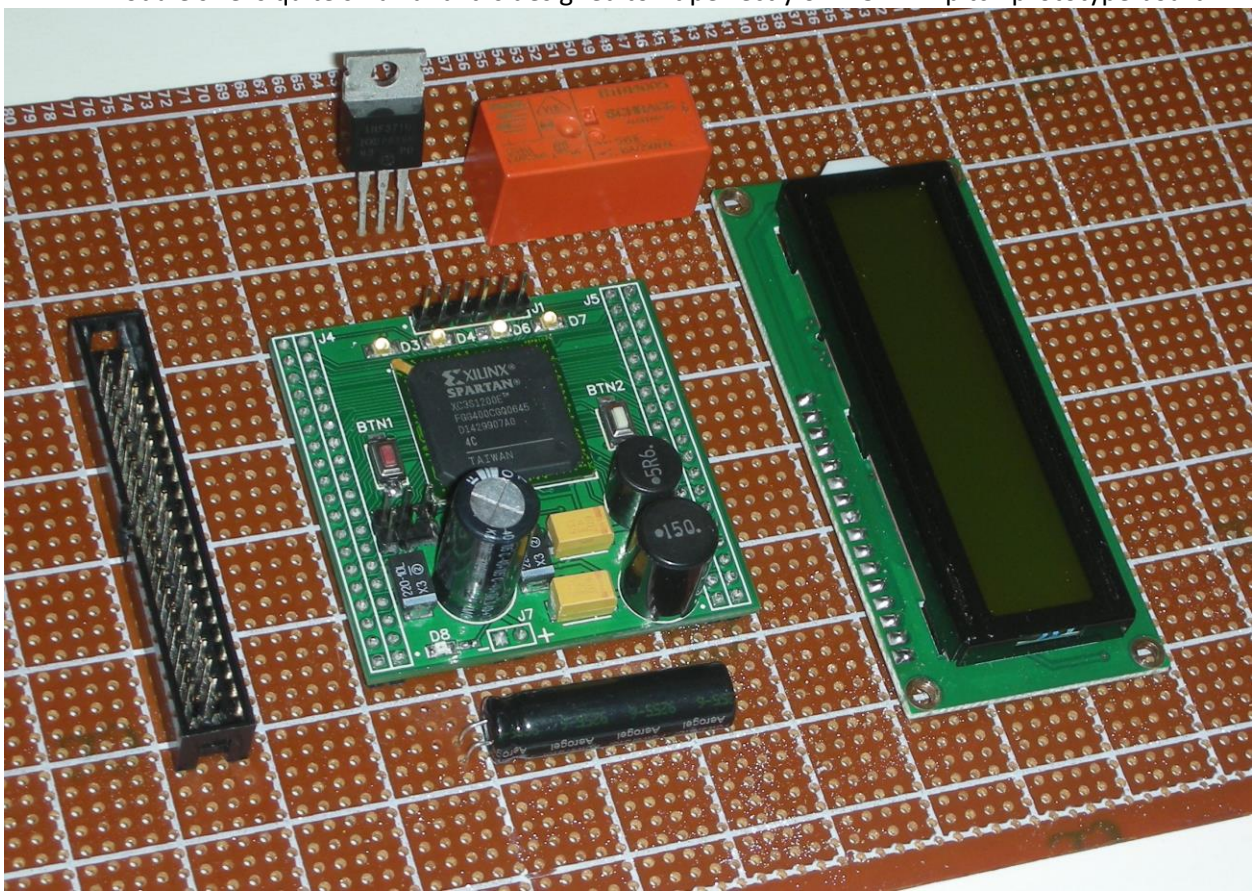
6) XMF3E module has triple-supply power management IC TPS75003 onboard. It is generating 3.3V, 2.5V and 1.2V supplies. 3.3V is used by FPGA IO, by onboard peripherals, and also supplied to IO connectors. 2.5V is used as FPGA VCCAUX and JTAG voltage. 1.2V is used as FPGA core voltage. Board also has LM1117 LDO, for generating 1.8V flash core voltage. D8 is a POWER-ON LED, when it lit - it means that there is input DC voltage connected. Input voltage range is 3.5V to 6.5V. Voltage, what is higher than 6.5V, can damage the board. If voltage, lower than 3.5V, is connected, and 3.3V cannot be properly generated, then MAX809 reset supervisor will hold PROG_B signal low. This will hold FPGA in reset mode.

- TPS75003 datasheet:
  http://www.ti.com.cn/cn/lit/ds/symlink/tps75003-ep.pdf
- LM1117-1.8 datasheet:
  http://www.ti.com/lit/ds/symlink/lm1117-n.pdf

7) There are total 76 I/O pins, what are routed to the connectors, and can be used in your design. Please refer to the board schematics, to get information about connections. All I/O are independent and not crossing with any boards peripherals. J3, J4, J5 and J6 are 19x1 male connectors. Each connector has 18 IO, 1 VCC 3.3V or 1 GND. Please note that all FPGA banks are powered from 3.3V, it means that you must use I/O standard “LVCMOS33” or “LVTTL” in your designs, to achieve better results. Please note that HSWAP pin is connected to VCC 3.3V, this means that when FPGA is not configured, all IO pull-up resistors are disabled. Please note that FPGA mode select pins become regular IO, after configuration process is finished, and can be used in some designs. Zip archive, for this board, will contain two ISE projects. First project is LED blink demo, what will be stored to flash. Second project is for testing IO pins. When IO test project is loaded, use fly wire, to connect IO pins one by one to VCC 3.3V. Test is passed if LEDs turn on, every time when one of IO pins is connected to VCC. Mode pins and IO button have hardware pull up resistors, so they are tested by connecting to GND. If there is missing contact

or short circuit between IO, LEDs will not turn on. Be careful, and don't make short circuit between VCC and GND.

Module size is quite small and it is designed to fit perfectly on 2.54mm pitch prototype board.



Powering up the board for the first time

1) Connect 5v to J7, with correct polarity.
2) Demo design will be automatically loaded into the FPGA, from the Flash, if all mode jumpers are installed.
3) IO LEDs will start blinking. This process can be adjusted with button BTN2.