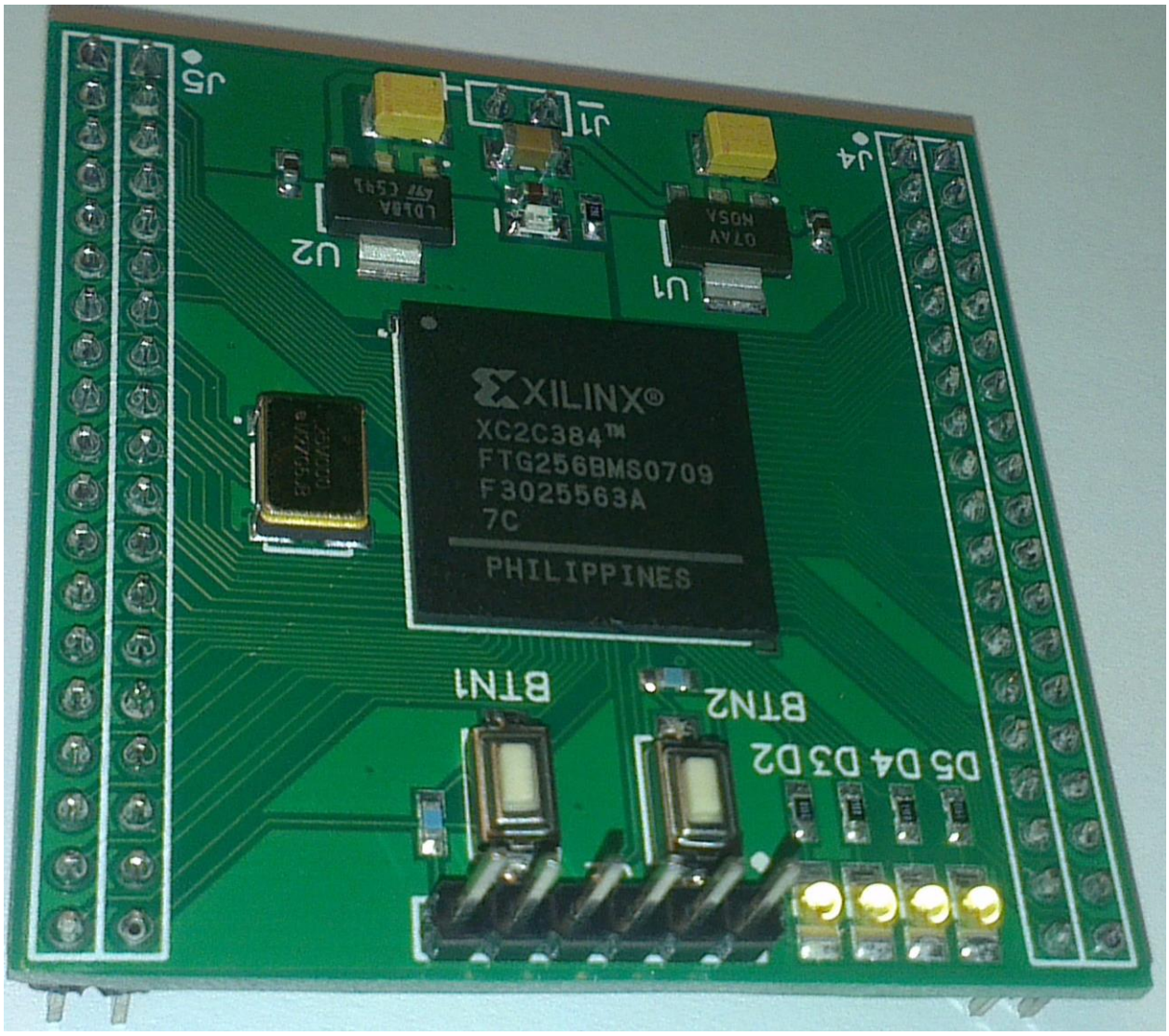
XILINX COOLRUNNER-2 CPLD MODULE USER's GUIDE

MODEL: XM2C2-384 Revision A



Introduction

XILINX COOLRUNNER-2 XM2C2-384 CPLD module is a low cost and easy to use tool. Designed for rapid prototyping and implementing CPLD designs. This module can be used independently, for education, or can be used as core module, for a bigger design.

Features

1) XILINX XC2C384 FTG256 7C CPLD
- 384 Logic Cells
- Maximum system frequency – 217 MHz
- On-The-Fly Reconfiguration (OTF)
- IEEE1149.1 JTAG Boundary Scan
- Flexible clocking modes
- Advanced design security
- Open-drain output option for Wired-OR and LED drive
- Optional bus-hold, 3-state or weak pullup on select I/O pins
- Guaranteed 1,000 program/erase cycles, 20 year data retention

2) Onboard IO peripherals
- 4 LEDs
- 2 push buttons
- 25 MHz CMOS crystal oscillator

3) Handy configuration
- Onboard JTAG header

4) Onboard power supply
- Input voltage range 5V – 15V
- 3.3V LDO
- 1.8V LDO
- POWER-ON LED

5) 72 independent I/O routed to the connectors
- Four 1x19 male connectors (18 IO, 1 VCC or 1 GND)
- 2.54mm pitch for all connectors
- 3.3V IO voltage
- Small 50x50mm PCB designed to fit on the prototyping board with 2.54mm pitch

Instructions

1) This board has XC2C384 FTG256 7C CPLD (256 ball package, speed grade 7, commercial temperature range 0°C to +70°C). The CoolRunner-II 384-macrocell device is designed for both high performance and low power applications. This lends power savings to high-end communication equipment and high speed to battery operated devices. Due to the low power stand-by and dynamic operation, overall system reliability is improved.
- CoolRunner-II CPLD Family datasheet: http://www.xilinx.com/support/documentation/data_sheets/ds090.pdf
- XC2C384 CoolRunner-II CPLD datasheet: http://www.xilinx.com/support/documentation/data_sheets/ds095.pdf

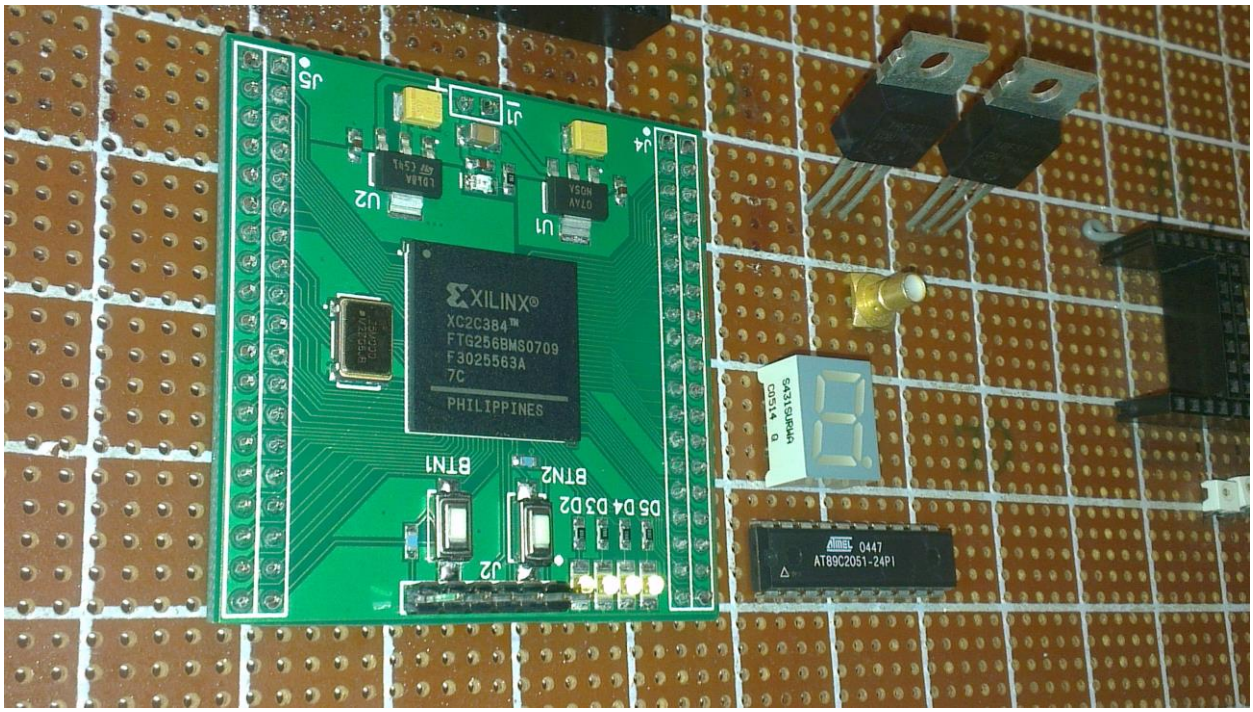
2) Board has few simple peripherals onboard: 4 yellow LEDs, 2 momentary active-low push buttons with pull up resistors. XM2C2 module is equipped with 25 MHz CMOS oscillator, what is connected to pin M2.

3) J2 is JTAG header, with 2.54mm pitch. Use JTAG-USB or JTAG-LPT cable, to program CPLD. JTAG signals have 3.3V voltage levels.

4) XM2C2 module has two LDOs onboard. 3.3V is generated by U1. 1.8V is generated by U2. 1.8V is used as CPLD core voltage. 3.3V is used for everything else. D1 is a POWER-ON LED, when it lit - it means that there is input DC voltage connected. Input voltage range is 5V to 15V. Voltage, what is higher than 15V, can damage the board.

5) There are total 72 I/O pins, what are routed to the connectors, and can be used in your design. Please refer to the board schematics, to get information about connections. All I/O are independent and not crossing with any boards peripherals. J3, J4, J5 and J6 are 19x1 male connectors. Each connector has 18 IO, 1 VCC 3.3V or 1 GND. Please note that all CPLD banks are powered from 3.3V, it means that you must use I/O standard “LVCMOS33” or “LVTTL” in your designs, to achieve better results. Zip archive, for this board, contains ISE project. It is test demo, what is programmed to CPLD during manufacturing. When board is powered on, with programmed test project, LEDs will blink. Blinking can be adjusted with buttons. Use fly wire, to connect IO pins one by one to GND. All LEDs will turn on, every time when one of IO pins is connected to GND. If there is missing contact or short circuit between IO, LEDs will be blinking. Be careful, and don’t make short circuit between VCC and GND.

Module size is quite small and it is designed to fit perfectly on 2.54mm pitch prototype board.



Powering up the board for the first time

1) Connect 5v to J1, with correct polarity. Red LED D1 should turn on.
2) Demo design will be automatically loaded by CPLD.
3) IO LEDs will start blinking. This process can be adjusted with buttons, or by connecting one of the I/O pins to GND.
4) Use XILINX ISE design suite, to create and compile your project.
5) Use XILINX “iMPACT” program, and compatible JTAG cable, to upload compiled project in to CPLD. You can also use JTAG cables what are not supported by “iMPACT”, with third party software.